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DEVELOPMENT AND CHARACTERIZATION OF INSULATING LAYERS ON SILICON CARBIDE: ANNUAL REPORT FOR FEBRUARY 14, 1988 TO FEBRUARY 14, 1989

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Processes to fabricate metal-insulator-semiconductor (MIS) capacitors on the cubic (3C) form of silicon carbide (SiC) were studied. The insulating layers were formed from either thermally grown oxide or chemical-vapor-deposited (CVD) silicon dioxide. The effects of wet or dry oxygen and of oxidation temperatures between 1050 and 1200 °C on the electrical properties of devices with thermal oxides were determined. Various post-oxide deposition thermal treatments were investigated for CVD oxide layers. Capacitors with CVD oxide layers that were annealed in nitrogen and subject to a short wet oxidation, and alloyed after metallization, had nearly the same electrical properties as capacitors with thermal oxides. Electrical characterization techniques appropriate for these devices on SiC were developed and applied to the fabricated capacitors. The capacitors were characterized from multiple-frequency capacitance-voltage (C-V) measurements as a function of temperature from room temperature to 300 °C. The apparent interface trap level densities were estimated from the high-frequency C-V curves. The C-V characteristics of SiC MIS capacitors have several distinctive features: (1) the capacitance decreases with increasing negative voltage into deep depletion; (2) at fields of about 2.5 x 10^6 V/cm, the capacitance recovers from deep depletion to its equilibrium inversion level; and (3) on the reverse sweep, a stagnant inversion layer is seen. From the analysis of the high-frequency C-V curves, the following electrical properties of typical capacitors (both thermal and CVD oxides) were determined: equivalent fixed charge, N_f, of 5 to 9 x 10^{11} cm^{-2}; interface trap level density at mid-gap, D_{it}, of 0.5 to 2.0 x 10^{11} $cm^{-2}eV^{-1}$; and oxide breakdown fields, V_{bd}, of 4 to 6 x 10^6 V/cm.

Key Words: capacitance-voltage measurements; compound semiconductors; interface trap level density; MIS capacitors; MOS capacitors; semiconductor processes; silicon carbide

Disclaimer

Certain commercial equipment, instruments, or materials are identified in this paper in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by NIST, nor does it imply that the materials or equipment identified are necessarily the best available for the purpose.

1. INTRODUCTION

The work described in this report was done for the National Aeronautics and Space Administration (NASA), Lewis Research Center, under NASA Lewis Order No. C-30007-K, for the period February 14, 1988 to February 14, 1989. The program is entitled "Development and Characterization of Insulating Layers on Silicon Carbide." The work is continuing under NASA Lewis Order No. C-30018-M.

Silicon carbide is a semiconductor with several attractive properties for electronic devices. These include a large band gap (2.2 eV in 3C SiC), high thermal conductivity, and high breakdown field, as well as excellent physical stability. Due to these electronic and physical properties, silicon carbide has long been known as an attractive material for high-temperature, high-frequency, and high-power electronic devices [1]. SiC-based electronics would have potential aerospace and space applications [2]. The development of SiC electronics has been limited due to the difficulty in growing high-quality, large-area crystals. One promising technique is the growth of single-crystal layers of the cubic (3C) form of SiC on silicon substrates by chemical-vapor deposition (CVD) processes [3]. The SiC used in this work was grown by this technique.

One possible SiC-based electronic device is the MISFET (Metal-Insulator-Semiconductor-Field-Effect-Transistor). MISFETs consist of doped source and drain regions and an MIS capacitor to control the conductivity of the channel between them. For MISFETs to take full advantage of the desirable properties of SiC, the process to fabricate MIS capacitors and their electrical characteristics must be well understood. This report presents the results of a study of the processes that form dielectric insulating layers on SiC and how these processes affect the electrical characteristics of MIS capacitors that these insulators partially form.

The objectives of the work were: (1) to fabricate MIS capacitors with grown or deposited insulators and deposited metal field-plates and substrate contacts; (2) to investigate different materials for the insulating layer and to vary the parameters of their formation to optimize the process; (3) to develop electrical measurement techniques to characterize the devices and the material; and (4) to apply these techniques to determine the electrical characteristics of the fabricated devices, including their behavior as a function of temperature up to 300 °C.

Previous studies have demonstrated that MIS capacitors on SiC could be made with capacitance that changed with voltage. Capacitors on both 6H (hexagonal) and 3C (cubic) SiC with thermal oxides have been reported from Kyoto University [4-6]. There is also a report of capacitors on CVD 3C SiC with wet thermal oxides utilizing mercury-probe contacts [7]. These reports dealt with a limited number of oxidation conditions and devices and mostly demonstrated feasibility. This study of MIS capacitors examines a wider range of processes and their effect on electrical characteristics.

A total of 18 different process variations to fabricate MIS capacitors were investigated. Both thermal oxides and CVD oxides were used as the insulating layer. The effect of thermal oxide growth temperature, oxidizing medium, and

post-oxidation annealing were investigated. All CVD oxides were deposited using the same deposition procedure. The effects of various post-deposition thermal treatments on the electrical characteristics of these devices were then investigated.

The devices were electrically characterized from their capacitance-voltage characteristics, oxide conductances, and breakdown voltages. The effect of the measurement frequency, voltage sweep rate, illumination, and temperature on the C-V characteristics was determined. Interface trap density was estimated from the high-frequency C-V curves using the Terman method [8].

2. MIS CAPACITOR FABRICATION

2.1 Starting Materials

The starting materials for this study were 3C SiC CVD epitaxial-layers grown on p-type silicon substrates [3]. Samples were grown at NASA Lewis Research Center. The electrical properties of the crystals were reported as: resistivity, from four-probe measurements, between 0.15 to 2.3 Ω-cm; the electron mobility, determined from Hall effect measurements, between 150 to 300 cm^2/Vs; and the electron carrier concentration, n, between 6 and 20 x 10^{16} cm^{-3}. The dimensions of the SiC layers were 1 cm x 1 cm with thicknesses of about 10 μm.

The heteroepitaxial growth of 3C SiC on (001) silicon results in SiC which has anti-phase boundaries (APBs). APBs result when SiC islands with different stacking sequences merge during the growth of the SiC layers. Growth of SiC on silicon which is tilted 0.5° to 4° toward the (110) plane eliminates APBs in SiC [9]. The SiC used in this study was grown on silicon substrates that were both on-axis and off-axis. SiC grown on-axis contains APBs and is denoted as such in the data presented. The off-axis SiC was grown on silicon which was either 1° or 0.5° off-axis and should not contain APBs. Although attention was paid in the processing and the subsequent electrical characterization, no effects due to the existence of APBs were determined.

2.2 Insulator Candidates

There were several options for the preparation of insulating layers on SiC. It was known that a thermal oxide with adequate electrical properties could be grown on SiC. Suitable oxides would exhibit sufficiently low surface charges and high enough dielectric strength that the surface could be inverted by the gate voltage. Since the properties of capacitors fabricated from only a limited number of oxidation conditions have been reported, one objective of this study was the investigation of oxide growth conditions on the electrical properties of MIS capacitors.

Auger electron spectra of the thermal oxide grown on SiC have shown it to be near stoichiometric silicon dioxide with less than one percent carbon content. An interfacial layer between the oxide and the SiC, containing substantial carbon and with a thickness of about 100 Å, has also been observed [4-6,10]. It is hypothesized that the growth mechanism of thermal oxide on SiC is due to the diffusion of the oxidant to the interface and the outward diffusion of CO through the oxide [10]. The presence of carbon at the interface and the possible existence of traces of carbon within the bulk of the oxide suggested

that deposited insulating layers (which would not contain residual carbon) could have superior electrical properties.

The process for the production of chemical-vapor-deposited (CVD) silicon dioxide and CVD silicon nitride insulators is readily available. Recent reports of capacitors and transistors on silicon [11] and gallium arsenide [12] with CVD oxide as the gate material suggests that the use of a deposited oxide as the insulating layer on SiC may be feasible.

Deposited nitrides on silicon [13] and on SiC [14] have been shown to have properties that make them undesirable for the gate insulator in an MIS capacitor. Their poor performance as gate insulators results from conduction through the nitride and flatband voltage shifts due to electron injection/trapping. Silicon nitride does, however, have properties such as a greater dielectric constant and potentially greater electrical and physical stability at higher temperature, that are superior to silicon dioxide for a gate insulator. An oxide-nitride-oxide structure has been shown to improve insulator performance [15]. Since this is a relatively complex process and depends on the formation of a good oxide-SiC interface, it was decided to concentrate the work on deposited oxides.

2.3 Device Geometries and Process Sequence

The mask set used to define the MIS capacitor dimensions is illustrated in figure 1. After insulating layer formation, 200-μm-diameter contact openings spaced 760 μm apart are made in the insulator. These openings are covered with 305-μm-diameter aluminum (1.5% Si) metal dots spaced 380 μm apart. Since the aluminum dots are spaced twice as densely as the contact openings, between each contact to the substrate are Al field-plates over oxide. The Al field-plate over oxide combined with an Al contact to the SiC forms an MIS capacitor. There are about 340 pairs of field-plates and contacts per square centimeter of SiC.

The goal for the insulator thickness was 800 Å. Actual insulator thicknesses depended on the process. For wet thermal oxides grown at 1100 °C for 3 h, the oxide thickness determined from the oxide capacitance was between 750 and 820 Å. Three separate CVD oxide deposition runs with slightly different thicknesses were made. Because the SiC substrates were sometimes shielded from the deposition gas, the thicknesses of the deposited oxide layers varied greatly. Deposited oxide from all deposition runs varied in thickness between 380 and 760 Å.

The Al (1.5% Si) metal over both the contacts and the insulator was 700 nm thick. The dc resistance from one Al contact through the SiC to the next nearest Al contact was measured as about 200 Ω (for SiC #820-2) with a linear I-V characteristic. This is approximately twice the series resistance of the MIS capacitors. The specific contact resistivity of the aluminum (1.5% Si) to n-type SiC (#820-10) was measured utilizing an array of lithographically fabricated contacts [16]. This technique is fully described and demonstrated for Al (1.5% Si) to silicon contacts in reference [16]. The essence of the technique is to subtract the calculated spreading resistance from the measured two-probe resistance leaving the resistance due to contact resistivity.

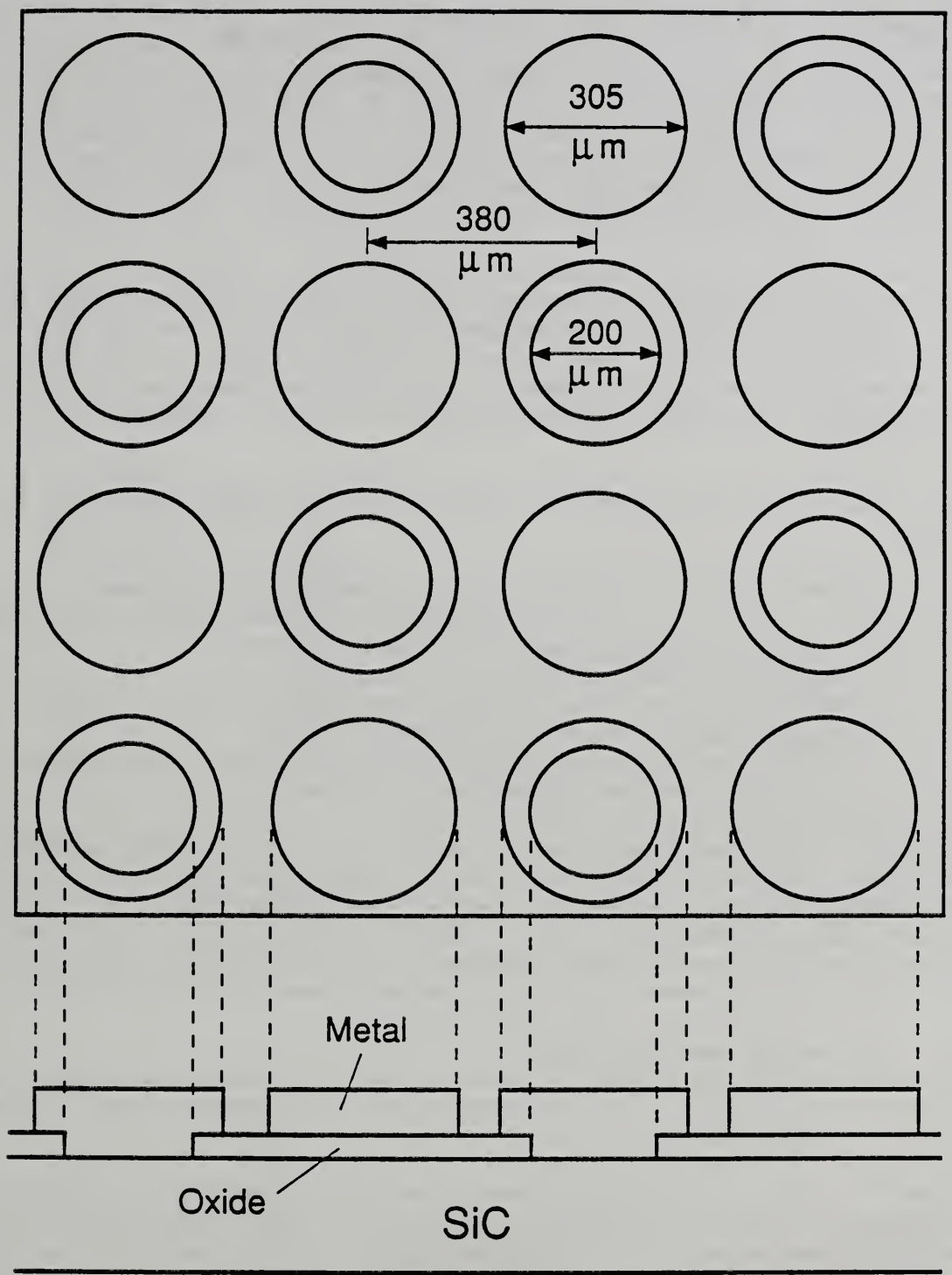

Figure 1. Capacitor geometries. Field plates are 305 μm in diameter and are evaporated aluminum with 1.5% Si, contact openings through the insulator to the SiC are 200 μm in diameter and are also covered by 305-μm-diameter aluminum contacts.

The two-probe resistance of the SiC substrate was measured as 1084 Ω at a probe spacing of 40 μm and ±0.01 mA of current. The four-probe resistance was measured as 181 Ω at a probe spacing of 40 μm and ±0.1 mA of current. The resistivity was calculated to be 0.82 Ω-cm based on a SiC thickness of 10 μm. The spreading resistance was calculated as 878 Ω based on the determined resistivity, a measured contact diameter of 9.0 μm, and an assumed ring delta current distribution through the contact. This indicates that the contact resistance is 206 Ω and that the specific contact resistivity for Al (1.5% Si) contacts to SiC (n-type with 0.82 Ω-cm resistivity) is 6.5×10^{-5} Ω-cm^2.

The uncertainty in this measurement technique is dominated by the error in determining the contact diameter. This is typically about 10%. The error in the contact resistivity is approximately proportional to the error in the contact area. An additional error is present in this measurement due to the uncertainty in the SiC thickness. It should be noted, for any future applications, that the contact resistivity will be dependent on the SiC resistivity.

The complete processing sequence used for the SiC MIS capacitors is described below:

1. Cleaning in 1:1:4 $NH_4OH:H_2O_2:H_2O$ at 80 °C for 20 min, 30 s, 2% HF acid dip, de-ionized water rinse
2. Insulating layer formation
3. Pre-metallization thermal treatments
4. Pattern and etch oxide to open contacts
5. Sputter deposit Al (1.5% Si) metal 700 nm
6. Pattern and etch metal to define field-plates and contacts
7. Post-metallization microalloying steps

In order to process these small (1 cm x 1 cm) crystals with semiconductor equipment designed to handle 7.5 cm or larger circular silicon crystals, the SiC crystals were attached to 7.5 cm silicon wafers with Apezion (black) vacuum wax. The crystals were attached to wafers after step 3 and removed after step 6. The wax used to attach the SiC to silicon substrates was resistant to all temperatures and chemicals used in the processing.

2.4 Insulating Layer Processes

Various thermal and deposited oxide processes to form insulating layers were investigated. Table 1 is a summary of all the processes used to fabricate MIS capacitors for this work.

There is little information in the literature regarding how the details of the processing affect the electrical properties of MIS capacitors of SiC. Post-oxidation annealing in Ar [4-6] and quickly pulling the SiC from the oxidizing medium into air [7] have been reported to improve capacitor characteristics. Wet oxidation has been reported to occur preferentially along dislocation bands resulting in a roughened surface after oxidation [17].

The procedure used here was the same for all thermal oxidations. Dry oxidations were done while flowing semiconductor-purity oxygen at 1500 cm^3/min. Wet oxidations were done while flowing oxygen at 1500 cm^3/min

TABLE 1 SUMMARY OF CAPACITORS FABRICATED

SiC ID#		Type of Insulator and Post-Deposition Treatment
		THERMAL OXIDES
820-2	(APBs)	Wet thermal, 1100 °C, 3 h
820-5		Wet thermal, 1100 °C, 3 h
916-6	(APBs)	Dry thermal, 1100 °C, 3 h
916-7		Dry thermal, 1100 °C, 3 h
975-5		Wet thermal, 1050 °C, 7 h
975-6	(APBs)	Wet thermal, 1100 °C, 3 h
975-8		Wet thermal, 1150 °C, 60 min
975-9	(APBs)	Wet thermal, 1200 °C, 26 min
919-8	(N doped)	Wet thermal, 1150 °C, 60 min
919-10	(N doped)	
931-5	(1° off-axis)	
931-6	(APBs, on-axis)	
977-6	(0.5° off-axis)	
977-9	(1° off-axis)	
986	(B doped epi on 981-8)	
		CHEMICAL-VAPOR-DEPOSITED OXIDES
820-4	(APBs) CVD Run #1	None
820-6		10 min at 1100 °C in wet oxygen
820-8		None
820-9		10 min at 1100 °C in nitrogen
820-10		None, contact array for measurement of Al-to-SiC contact resistivity
906-9	CVD Run #2	Pre-deposition, 30 min at 1000 °C in wet oxygen Post-deposition, 20 min at 1000 °C in nitrogen
906-10		Pre-deposition, 60 min at 1000 °C in wet oxygen Post-deposition, 20 min at 1000 °C in nitrogen
906-7		20 min at 1000 °C in nitrogen followed by 60 min in wet oxygen
916-9	(APBs)	20 min at 1000 °C in nitrogen followed by 30 min in wet oxygen
916-10		20 min at 1000 °C in nitrogen followed by 30 min in wet oxygen
931-7	CVD Run #3	20 min at 900 °C N_2, 120 min wet O_2
931-9	(APBs)	20 min at 1000 °C N_2, 90 min wet O_2
931-10		20 min at 1100 °C N_2, 10 min wet O_2
977-2	(0.5° off-axis)	20 min at 1150 °C N_2, 5 min wet O_2

and hydrogen at 2000 cm^3/min. The SiC crystals were placed flat on a quartz boat. The process gases were allowed to flow through the tube for a long enough time to establish equilibrium before the crystals were manually pushed into the furnace. After the desired oxidation time, the SiC crystals were removed from the furnace by quickly (about 10 s) pulling the boat into an extension on the mouth of the furnace tube. Process gasses were then turned off and replaced with 2000 cm^3/min of nitrogen. The crystals were allowed to cool before being removed from the extension of the tube.

Electrical data from SiC capacitors formed with thermally grown insulators are presented in table 1. The data are divided into three groups representing three experiments. The first group of four SiC substrates was a baseline experiment to determine the quality of capacitors that could be produced with a simple thermal oxidation process. It was found that wet oxides were substantially superior to dry oxides, in terms of fixed oxide charge.

The second group of four SiC MIS capacitors was to determine the effect of oxide growth temperature on the electrical characteristics of the devices. It is well known that growth temperature affects the ultimate quality of MOS capacitors on silicon. Wet thermal oxides were grown on SiC at temperatures of 1050, 1100, 1150, and 1200 °C for 7 h, 3 h, 1 h, and 26 min, respectively. Oxidation time was adjusted to produce approximately the same thickness of oxide (approximately 800 Å).

The third group of SiC MIS capacitors utilized representative crystals from different growth runs, with different doping, or varying silicon substrate orientation. These SiC substrates had oxides grown at the same time with a near optimum oxidation process (1100 °C in wet oxygen for 3 h). By growing an identical oxide layer on SiC crystals which were different, a variation in the electrical characteristics of the capacitor due to the SiC substrate properties should be obvious when the C-V curves are compared.

Deposited oxides for capacitors were formed by low-pressure, chemical-vapor deposition. This process used the reaction of silane and oxygen in a hot-wall reactor at 425 °C. The SiC chips were attached to vertical quartz sample holders using nichrome wire clips that had previously been coated with silicon dioxide. The deposition rate was approximately 30 Å/min.

The device characteristics were optimized in the post-deposition thermal treatments. Post-deposition treatments were intended to accomplish three distinct purposes: densification, oxidation, or microalloying. Densification or annealing was accomplished at high temperature in a nitrogen atmosphere. Densified oxides exhibit a slower etch rate in HF acid than those that have not been densified. Post-deposition oxidation treatments were carried out in wet oxygen. This was to grow a thin (<50 Å) layer of thermal oxide between the SiC and the deposited oxide. This kind of post-deposition treatment could combine the interfacial properties of a thermal oxide with the bulk oxide properties of the CVD oxide. The combination of densification in nitrogen followed by a short oxidation step has been shown to produce CVD oxide layers on silicon with excellent electrical properties [11]. Further details of the post-deposition treatments are included in table 1.

The final kind of post-deposition treatment, microalloying, sometimes called sintering, is a step after Al metal deposition at moderate temperatures (350-600 °C) in a hydrogen-containing ambient. In this work, 10% hydrogen, 90% nitrogen (forming gas) was used. This type of treatment results in significant improvement in the electrical characteristics of silicon MOS capacitors [18]. Microalloying experiments were tried on both thermal and CVD oxide capacitors after determining the nonalloyed electrical characteristics.

The CVD oxide capacitors in table 1 are also divided into three categories. The first group of capacitors were a baseline run to determine the properties of unannealed CVD oxides on SiC, both with APBs and without. Some capacitors in this group were exposed to a single post-deposition treatment at 1100 °C in either a oxygen or nitrogen atmosphere.

The second group of crystals represents an attempt to find a post-deposition treatment consisting of a densification step in nitrogen followed by a much shorter wet oxidation step to grow a thin, interfacial layer of oxide. Some of the second group of CVD capacitors with this combined densification and oxidation step had electrical properties of the same quality as thermal oxides.

The third group of CVD capacitors was an attempt to find the optimum temperature for the combined nitrogen densification and oxidation step. Four SiC crystals had identical oxide layers deposited at the same time, followed by densification and wet oxidation at 900, 1000, 1100, or 1150 °C.

3. ELECTRICAL CHARACTERIZATION

3.1 Criteria for Evaluation

The relative quality of each process used to fabricate an MIS capacitor was determined from the resulting device electrical characteristics. For an MIS capacitor, this commonly consists of measuring the capacitance as a function of voltage over such a range of voltage that the complete behavior of the device is seen. Additional information is obtained by also measuring the current-voltage characteristics of the device. A comprehensive reference describing an MIS capacitor's electrical behavior and techniques to characterize them is [18].

In order for an MIS capacitor to function as the gate insulator of an MISFET, it must be capable of inverting the conduction type of the surface of the semiconductor. This means that its C-V characteristic will display a transition from accumulation through depletion to inversion. Other electrical properties of MIS capacitors which determine how well suited the device is to function as a gate insulator are as follows:

(1) The insulating layers should have high dielectric strength (high-breakdown voltage) to support an electric field sufficient to invert the semiconductor surface and to survive the transient voltage spikes that may be encountered in normal circuit operation. The layers must also have good insulating properties (high resistivity) so that very little current flows through the gate during the operation of the transistor.

(2) The fixed charge and the charge trap density in the oxide and at the interfaces should be low and controllable. This allows the transistor to be turned on or off at a fixed low voltage. Large numbers of traps stretch out the C-V curve, necessitating larger voltage swings to change the state of the device and resulting in slower switching speeds.

(3) All the capacitor's properties should be stable under voltage stress and with temperature. This means that when the C-V characteristic is measured, little hysteresis should be seen between the forward and reverse voltage sweeps, and the same C-V curve should be measured each time.

3.2 Capacitance-Voltage Characteristics of SiC MIS Capacitors

The small-signal capacitance-voltage characteristics of the devices were measured using Hewlett-Packard HP-4274A or HP-4275A Multi-Frequency LCR Meters. These meters use an ac test signal to measure small-signal capacitance. Measurement frequencies from 100 Hz to 10 MHz were available. Usually, the ac signal was 15 mV. At frequencies below 1000 Hz, a slightly larger ac signal was used to reduce the noise. The dc voltage was applied as a step ramp. Voltage steps were controlled in increments of 100 mV, and the time between voltage steps was 200 ms or greater. By varying the step size and the time between steps, the effective voltage sweep rate was varied. Contacts to the Al field-plate and substrate contact were made with tungsten probes located with micro-positioners under a microscope. Temperature was controlled with a Temptronic TP-36 high-temperature chuck, which allowed rapid heating or cooling between room temperature and 300 °C. When noted, device illumination was provided by the 35-W microscope light focused to a 5-mm spot covering the device and the contact. Otherwise, the C-V characteristics were measured in a dark, shielded box.

The C-V curves were analyzed using the abrupt depletion region approximation [19]. From the high-frequency C-V characteristic, the oxide capacitance (the capacitance in strong accumulation) and the inversion capacitance were determined. From these two capacitances, the following quantities were calculated: the insulator thickness, T_{ox}, semiconductor type, net doping concentration, N_d, and the flatband capacitance, C_{fb}. The flatband voltage, V_{fb}, was determined as the voltage at which the calculated flatband capacitance occurred. The doping concentration determined in this manner was approximately proportional to the reported resistivity of the SiC.

The variation of the flatband voltage from zero, after taking into account the metal-semiconductor work function, is a gauge of the fixed charge density, N_f, at the semiconductor-insulator interface. The presence of interface trap charge can significantly distort N_f determined in this way. For the best thermal oxides, N_f was 5 to 9 x 10^{11} cm^{-2}. The values for CVD oxides varied widely depending on the post-deposition processing they received. For an as-deposited oxide, N_f was 30 to 40 x 10^{11} cm^{-2}. After certain post-deposition thermal treatments discussed below, the best CVD oxides were comparable to thermal oxides. N_f for the best CVD oxides was about 5 to 10 x 10^{11} cm^{-2}. A complete summary of device parameters determined from electrical measurements is presented in table 2.

At room temperature, MIS capacitors on SiC display several features that would

TABLE 2 SUMMARY OF DEVICE ELECTRICAL PROPERTIES

SiC ID#	Insulator	T_{ox} Å	N_d ($\times 10^{16}$) cm^{-2}	V_{fb} V	N_{fe} ($\times 10^{11}$) cm^{-2}	D_{it} ($\times 10^{11}$) $cm^{-2}eV^{-1}$
THERMAL OXIDES						
820-2*	Wet, 1150 °C	722-747	1.5-1.8	-2.6 -3.5	6.4- 8.9	0.7-1.4
820-5	Wet, 1150	811-826	0.7-0.8	-2.8 -4.7	6.4-10	0.9-1.8
(550 °C alloyed)		---	---	-3.8 -4.3	9.6-11	3.5-10
916-6*	Dry, 1150	580-605	C-V almost flat			
916-7	Dry, 1150	580-605	C-V almost flat			
975-5	Wet, 1050 °C	699	0.79	-3.5 -4.4	9.4-12	2.3
975-6*	Wet, 1100	694	1.53	-3.6 -4.6	9.8-13	1.8
975-8	Wet, 1150	605	0.90	-3.1 -4.4	9.6-14	2.4
975-9*	Wet, 1200	589	1.53	-4.2 -5.3	14-18	2.1
Wet thermal, 1100 °C, 3 h:						
919-8	(N doped)	680	10.9	-3.4 -3.6	9.6	8.8
919-10	(N doped)	683	15.0	-3.0 -3.3	8.4	4.1
931-5	(1° off-axis)	699	0.56	-3.2 -4.3	8.5-12	2.1
931-6*	(APBs, on-axis)	684	0.85	-3.1 -4.2	8.4-12	2.5
977-6	(0.5° off-axis)	696	1.02	-3.5 -4.4	9.7-12	2.5
977-9	(1° off-axis)	679	1.31	-3.1 -4.0	8.5-11	1.5
986*	(B doped epi)	750	960 (p-type)	-25 -30	75	
CHEMICAL-VAPOR-DEPOSITED OXIDES (RUN #1)						
820-4*	not densified	457-488	1.8#	-8.8	39	3.9
(450 °C alloyed)				-4.1	17	10
820-8	not densified	458-547	0.7#	-8.4	38	48
(450 °C alloyed)				-4.5	16	80
820-6	O_2 densified	615-687	1.0	-2.7	7.5	3.3
(450 °C alloyed)				-3.2 -3.8	12	1.8
820-9	N_2 densified	564-573	5.0#	-7.4	27	9.5-30
(450 °C alloyed)				-3.3	11	4.3
820-10	Contact array	---	---	---	---	---

TABLE 2 (CONTINUED)

SiC ID#	Insulator	T_{ox} Å	N_d ($\times 10^{16}$) cm^{-2}	V_{fb} V	N_{fe} ($\times 10^{11}$) cm^{-2}	D_{it} ($\times 10^{11}$) $cm^{-2}eV^{-1}$
CHEMICAL-VAPOR-DEPOSITED OXIDES (RUNS #2 and #3)						
906-7x	Dens/Ox at 1000 °C	---	---	---	---	---
906-9	Pre-dep oxide	694-700	1.2#	-14	42	>200
	(450 °C alloyed)			-19	58	9.9
906-10	Pre-dep oxide	751-763	1.2#	-8.6 -10	23 - 27	>100
	(450 °C alloyed)			-17 -18	47 - 50	4.0-7.7
916-9*	Dens/Ox at 1000	559-629	1.6	-4.9	16	1.5
	(450 °C alloyed)		1.2-1.6	-4.3 -5.9	15 - 19	0.5-2.0
916-10	Dens/Ox at 1000	544-580	2.2	-5.1 -5.6	17 - 19	5.0-11
	(450 °C alloyed)			-4.0 -4.7	14 - 17	1.8-7.0
931-7	Dens/Ox at 900 °C	385	0.9	-1.3 -2.0	5.2- 8.9	1.7
931-9*	Dens/Ox at 1000	408	0.7	-4.0 -4.9	19 - 24	2.3
931-10	Dens/Ox at 1100	413	1.5	-3.0 -3.1	13 - 14	1.2
977-2	Dens/Ox at 1150	432	1.2	-3.5 -5.0	16 - 24	2.3

Alloying was for 20 min in 10% hydrogen, 90% nitrogen forming gas.
All thermal oxides were alloyed at 450 °C.

* SiC containing APBs. SiC #977-2 and #977-6 are on 0.5° off-axis silicon, all other SiC are on 1° off-axis silicon and APB free.

x This process failed, deposited oxide very thin.

Inversion capacitance could not be precisely determined. Doping estimated from other SiC with same run #.

commonly be seen in silicon capacitors only at low (77 K) temperatures. A typical C-V characteristic for a silicon carbide MIS capacitor is shown as the solid line in figure 2. During the forward voltage sweep (from positive voltages in accumulation to negative voltages in inversion), the C-V curve goes into deep depletion. Deep depletion results when the minority carrier generation rate is too slow to follow the dc gate bias ramp voltage. No inversion layer can form, and the depletion layer increases beyond its thermal equilibrium width.

At the most negative voltages during the forward sweep, the C-V curve is seen to recover from deep depletion to the inversion capacitance. This has been explained as resulting from electron tunneling [7]. As the gate voltage is increased towards inversion, the energy bands bend upward. In the extreme, the quasi-Fermi level at the surface is bent above the value of the conduction band in the bulk. The high field causes electrons to be emitted from the interface traps. The electrons from interface traps can then tunnel through the depletion region to the conduction band. Electrons from the valence band can then hop into the empty traps, leaving holes behind.

During the reverse voltage sweep, the C-V curve displays a stagnant inversion layer [20]. This is also due to the low minority carrier recombination rate. As the gate voltage is swept towards accumulation, the amount of balancing charge in the underlying semiconductor must correspondingly be reduced. In silicon at room temperature, this would be accomplished by the charge in the inversion layer recombining. Since the recombination rate is very slow in SiC at room temperature, the charge is balanced by reducing the majority carrier charge in, and thereby the width of, the depletion layer. This results in a corresponding increase in the device capacitance above the inversion value. Similar effects have been observed in silicon at low temperatures [20].

The capacitors were found to be very light-sensitive. A C-V characteristic measured under illumination is also shown as the dashed line in figure 2. Under illumination, the capacitance does not go into deep depletion, but gradually approaches a constant value at large negative voltages. This value is noticeably higher than the equilibrium inversion value reached in the dark. This is consistent with what is observed with silicon MIS capacitors at low temperatures [20]. If after reaching equilibrium in the dark, light is turned on, the capacitance rises to a higher equilibrium value. If this light is removed, the capacitance gradually returns to the previous equilibrium value in the dark. The light serves to increase the steady-state carrier concentration in the inversion region above its thermal equilibrium value [21].

Little difference was seen in the C-V characteristics as a function of measurement frequency from 100 Hz to 1 MHz. At all frequencies, the capacitors still enter into deep depletion. Compared with a 1-MHz C-V curve, at frequencies of 10 KHz or less a small part of the curve in the depletion region was shifted toward more negative voltages. C-V curves at both 1 MHz and 100 Hz are shown in figure 3. This frequency dependence is due to interface traps responding to the ac signal.

The voltage sweep rate did not appreciably change the measured capacitance in

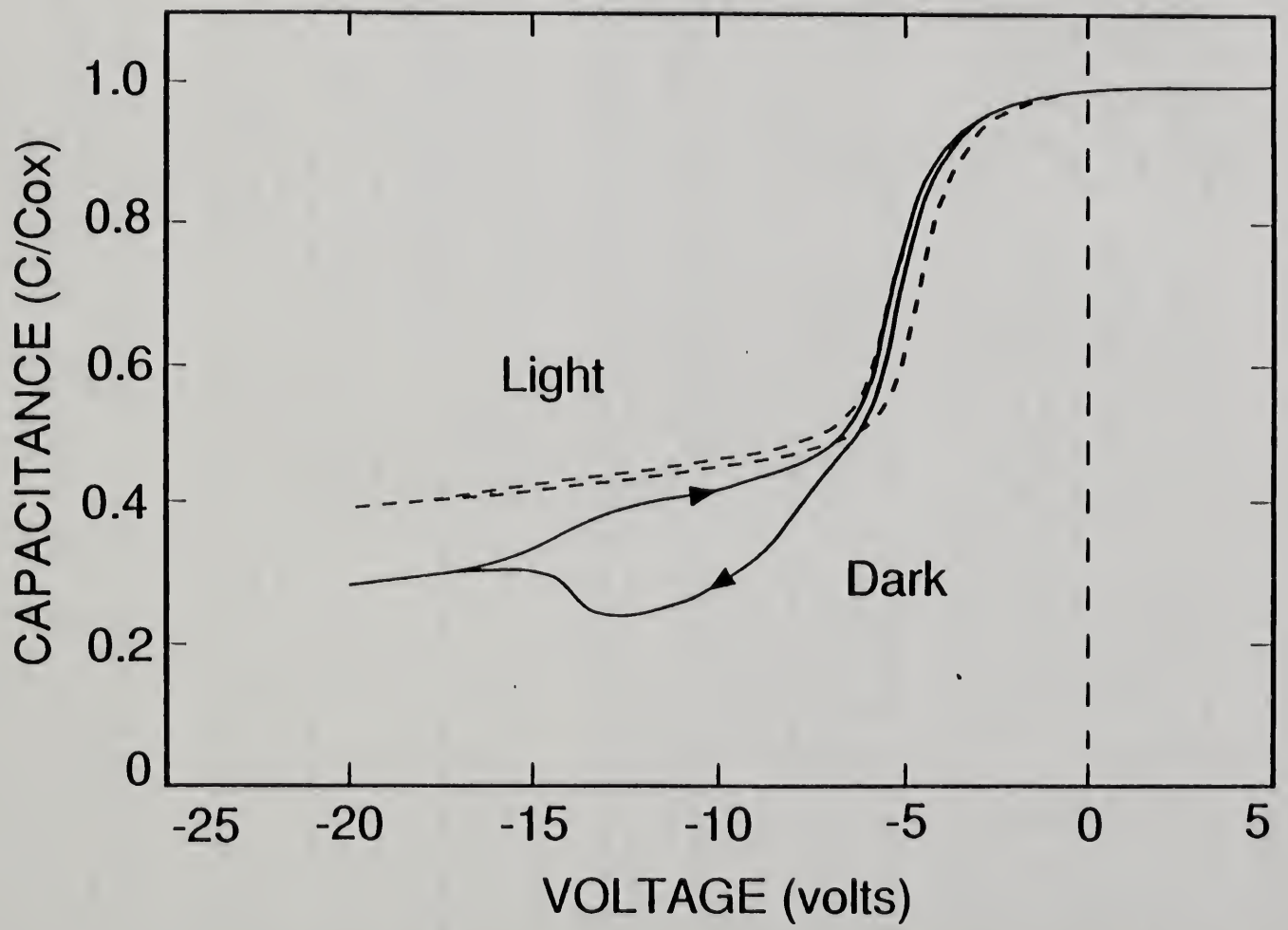

Figure 2. C-V curve for a capacitor with a wet thermal oxide insulating layer (#820-5), illustrating behavior typical for 3C SiC MIS capacitors. The solid line C-V curve was measured in the dark at very low sweep rates, 0.01 mV/s. The dashed line C-V curve is for the same device under illumination, sweep rate of 40 mV/s

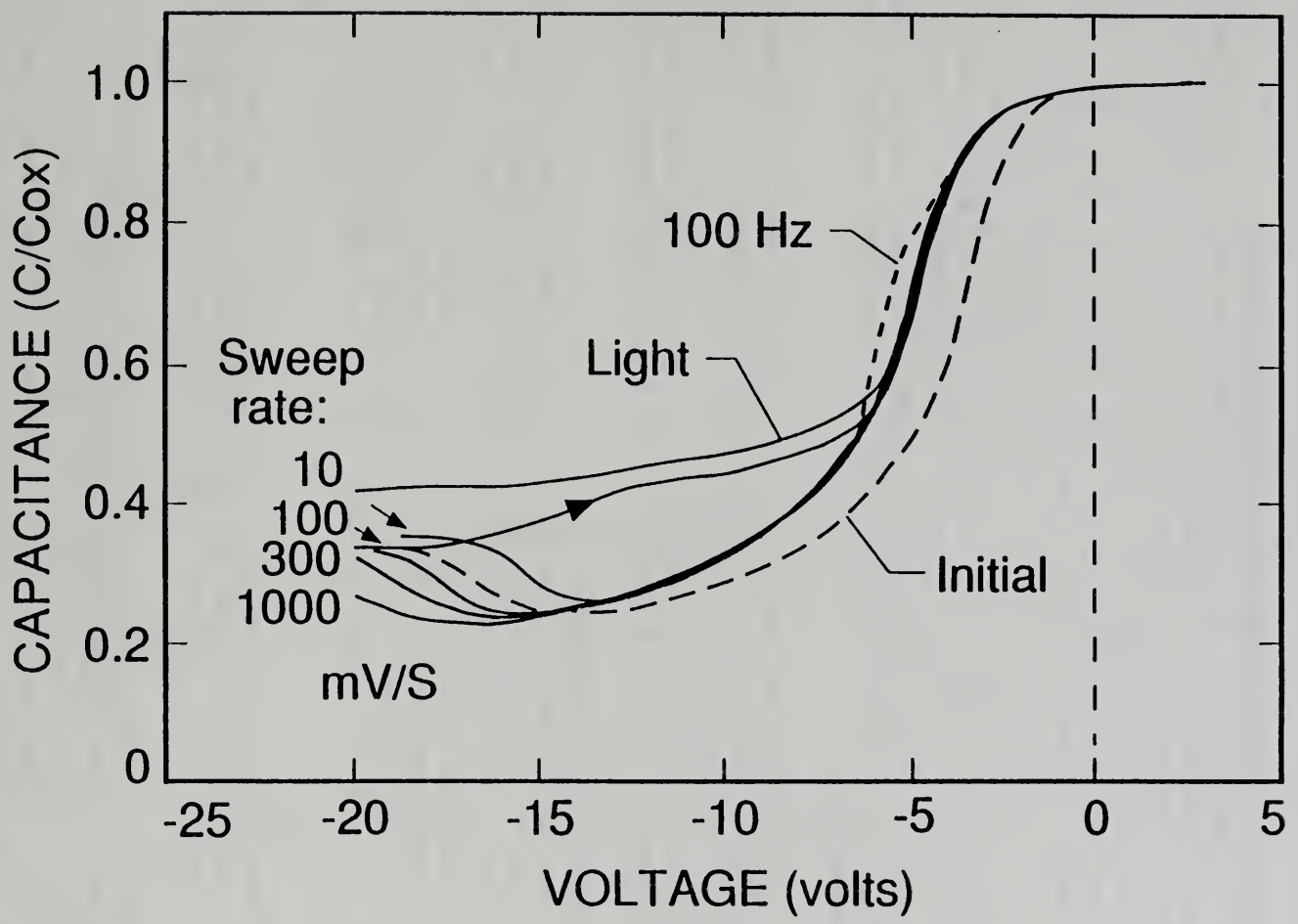

Figure 3. Effect of measurement frequency (100 Hz and 1 MHz) and sweep rate (10, 100, 300, and 1000 mV/s) on capacitor C-V characteristics. Little change is seen with measurement frequency. Sweep rate effects mostly the region of the C-V curve where recovery from deep depletion takes place. After the initial measurement, the C-V curve appears to shift about -1.5 V.

accumulation or depletion. Reducing the sweep rates reduced the voltage at which the capacitance would begin to increase from deep depletion. In figure 3, the 1-MHz C-V characteristic is shown at sweep rates of 10, 100, and 1000 mV/s. The minimum voltage at which recovery begins corresponds to a field of 2.5×10^6 V/cm across the oxide. If during either the forward or reverse sweep the voltage ramp is stopped, the capacitance will gradually relax to a constant value. This value is the thermal equilibrium value. At a large enough negative bias, this will be the inversion capacitance.

3.3 Effect of Temperature on C-V Characteristics

The C-V characteristics of SiC MIS capacitors were also determined as a function of temperature. Figures 4 and 5 show C-V curves for a thermal oxide capacitor at temperatures of 25, 130, 200, and 305 °C in the forward and reverse directions, respectively. The voltage at which the capacitance began to recover from deep depletion and the voltage at which the capacitance reached equilibrium both decreased with increasing temperature. Most thermal and some CVD oxides were found to have sufficient dielectric strength to operate to at least 300 °C. At 300 °C, a true high-frequency C-V characteristic is seen; i.e., the capacitance decreases steadily through depletion until reaching a constant value in inversion. Deep depletion no longer occurs at this temperature. Similar to the case of illumination, the inversion capacitance at 300 °C is higher than the inversion capacitance at room temperature.

As the temperature was increased, the location of the flatband voltage, and thus the fixed charge density, appeared to increase. For the C-V curves in figure 4, the fixed charge density was 8, 11, 14, and 16 x 10^{11} cm^{-2} at 25, 130, 200, and 305 °C, respectively. After the high-temperature cycle, the C-V characteristic returned to near the original room-temperature characteristic.

3.4 Comparison of Processes

Comparisons of thermal oxides: The initial wet thermal oxides grown at 1100 °C for 3 h on #820-2 and #820-5 were of high quality and displayed a recovery from deep depletion to inversion. This recovery requires a high field across the insulator and, therefore, indicates a high-quality oxide. The C-V curve obtained for this process is shown in figure 2. The minimum value of N_f was 6 x 10^{11} cm^{-2}, D_{it} (at mid-gap) was 0.5 x 10^{11} cm^{-2} eV^{-1}, and V_{bd} was about 5 x 10^6 V/cm. These values are adequate for device applications.

The oxides grown in dry oxygen, #916-6 and #916-7, were much inferior to wet oxide. The transition from the oxide capacitance to depletion only began to occur at about -20V, indicating very high fixed and interface trap densities.

The effect of oxide growth temperature on the C-V characteristic was determined by growing oxides in wet oxygen at 1050 °C for 7 h, 1100 °C for 3 h, 1150 °C for 1 h, and 1200 °C for 26 min on SiC #975-5, #975-6, #975-8, and #975-9, respectively. The C-V curves of these four capacitors are presented in figure 6. The C-V curves measured for these oxides are very similar. While the oxide thicknesses and doping densities are different, the fixed charge and interface trap densities are almost identical. Fixed charge for oxides grown between 1050 and 1150 °C was about 9 x 10^{11} cm^{-2}. Only the

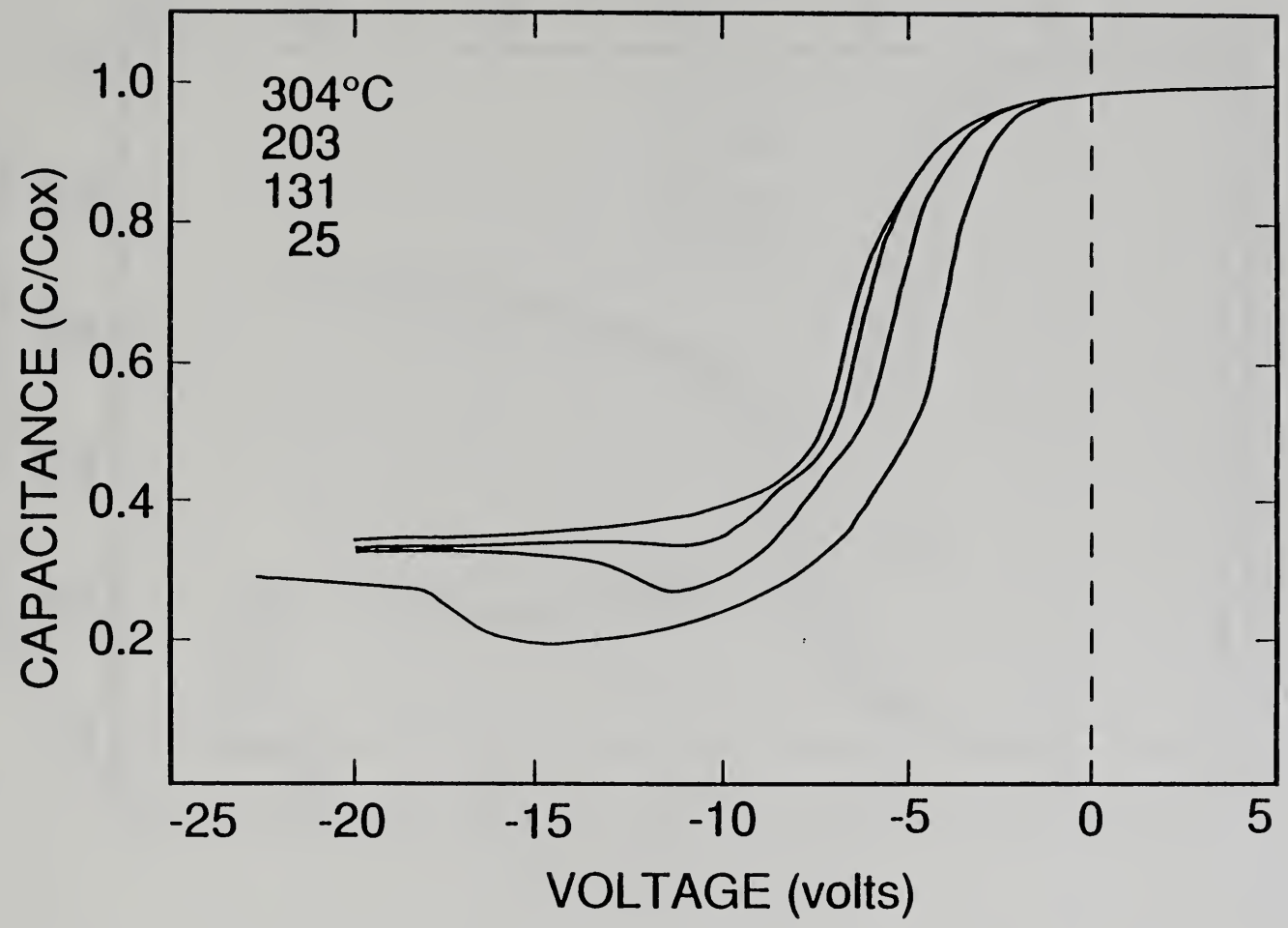

Figure 4. Effect of temperature on the C-V characteristic when swept in the forward direction. Curves are for 25, 130, 200, and 300 °C.

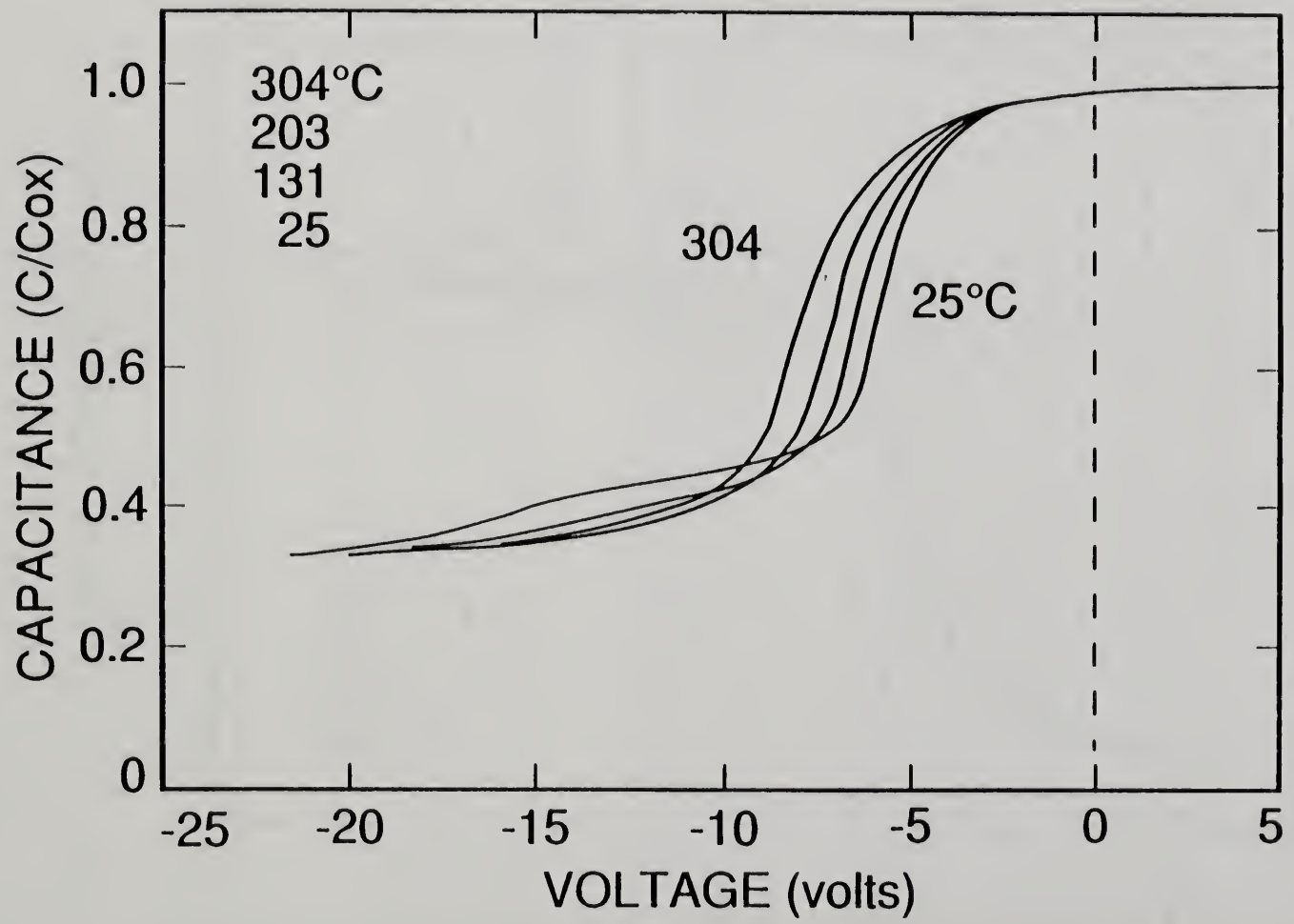

Figure 5. Effect of temperature on the C-V characteristic when swept in the reverse direction. Curves are for 25, 130, 200, and 300 °C.

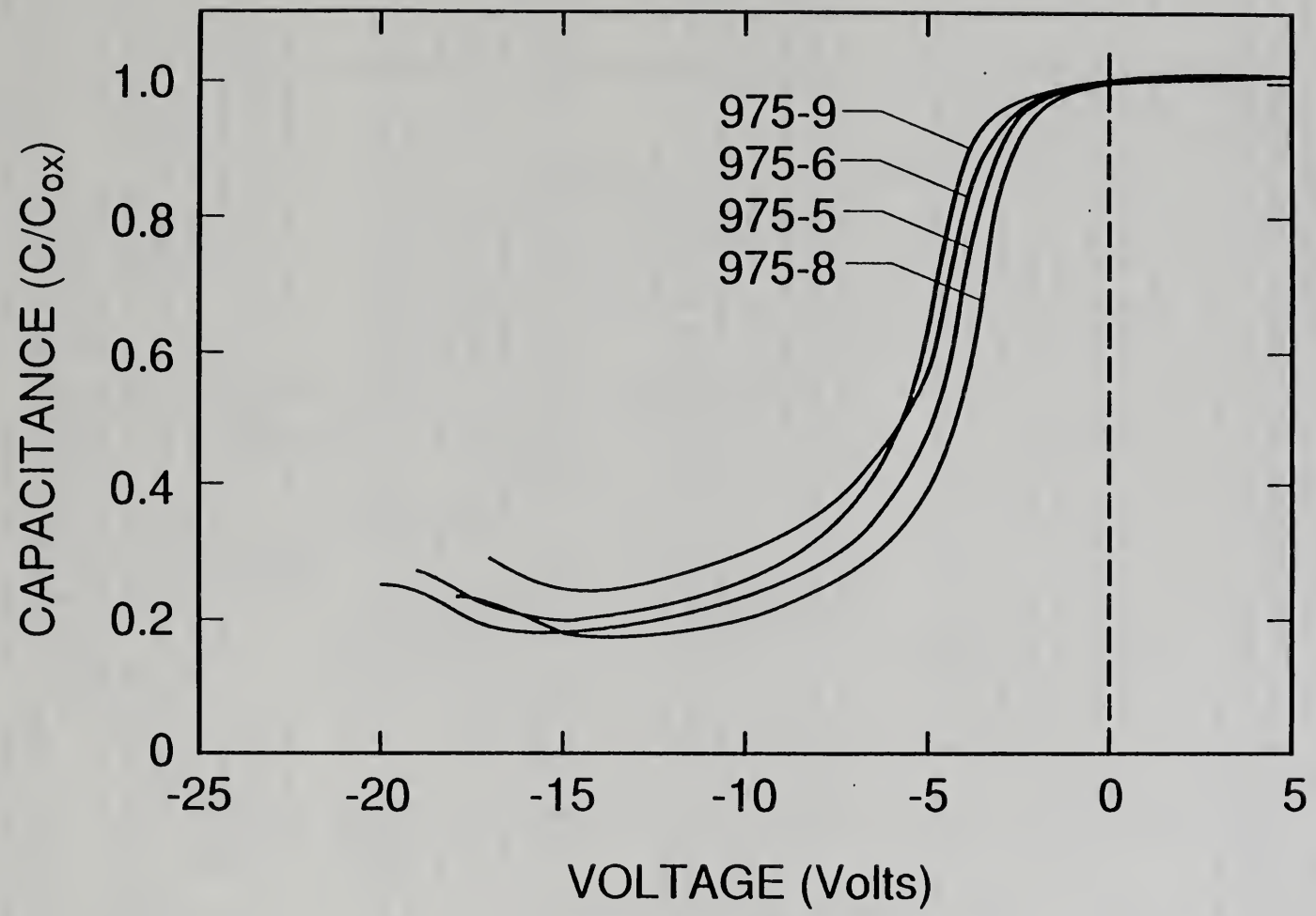

Figure 6. C-V characteristics of capacitors with wet thermal oxide insulating layers. Oxides were grown at temperatures of 1050, 1100, 1150, and 1200 °C. Oxidation times were adjusted to produce approximately the same oxide thickness. Capacitors were alloyed at 450 °C in forming gas after metal deposition.

oxide grown at 1200 °C had a slightly higher fixed charge at about 14×10^{11} cm^{-2}. These results indicate that the oxide growth temperature is not a limiting factor. It could be another step in the process, such as the post-metallization microalloying step, that controls the final magnitude of the oxide charges.

Comparisons of densifying steps of CVD oxides: A comparison of the C-V curves obtained for capacitors with CVD oxides and various thermal treatments is included as figure 7. These devices had not yet been subject to a post-metallization alloying step. Before alloying, all CVD oxide capacitors had fixed oxide charge and interface trap density greater than wet thermal oxides.

Initially, four SiC crystals had CVD oxides deposited on them. As-deposited CVD oxides, #820-4 and #820-8, had fixed charge densities about an order of magnitude greater than wet thermal oxides, went into deep depletion, but did not recover before the oxide broke down. The CVD oxides on SiC #820-6 and #820-9 received a single post-deposition treatment at 1100 °C for 10 min in wet oxygen or nitrogen, respectively. The wet oxygen appeared to be much more effective in reducing fixed oxide charge. Both of these high-temperature densifying steps greatly increased the CVD oxides resistance to etching in HF acid.

The second group of SiC to have CVD oxides deposited on them was subjected to combined densification in nitrogen followed by a short wet oxidation step. Growing the thin thermal oxide before deposition was tried on #906-9 and #906-10. These were oxidized at 1000 °C in wet oxygen for 30 and 60 min, respectively. After oxide deposition, they were densified in nitrogen at 1000 °C for 20 min. These pre-deposition oxidized SiC had poor C-V curves. The thermal oxide may have been degraded by the subsequential oxide deposition process.

Subjecting the deposited oxide to an oxidation step post-deposition was more effective. SiC #916-9, #916-10, and #906-7 were subject to post-deposition densification in nitrogen for 20 min, followed immediately by oxidation in wet oxygen at 1000 °C for 30, 30, and 60 min, respectively. SiC #906-7 failed, due to a very thin deposited oxide. Both #916-9 and #916-10 had much lower fixed charge and trap densities than the as-deposited oxide capacitor. None of the first or second group of CVD oxides showed a recovery from deep depletion before alloying.

All of the CVD capacitors fabricated in the first two batches were alloyed at 450 °C in forming gas for 20 min. The C-V curves of the same capacitors in figure 7 are shown in figure 8 after alloying. All the capacitors showed a dramatic "sharpening" of the transition from accumulation to depletion, indicating a reduction of interface traps. The fixed charge densities are also apparently reduced. This is not always reflected by the values reported in table 2, due to changes in the shape of the C-V curve from trap charge.

After alloying, three of the CVD oxides, #820-6, #916-9, and #916-10, displayed a recovery from deep depletion. Capacitors with this feature have oxides which can support a greater electric field than those that do not. All of these capacitors had been subjected to a post-deposition oxidation step.

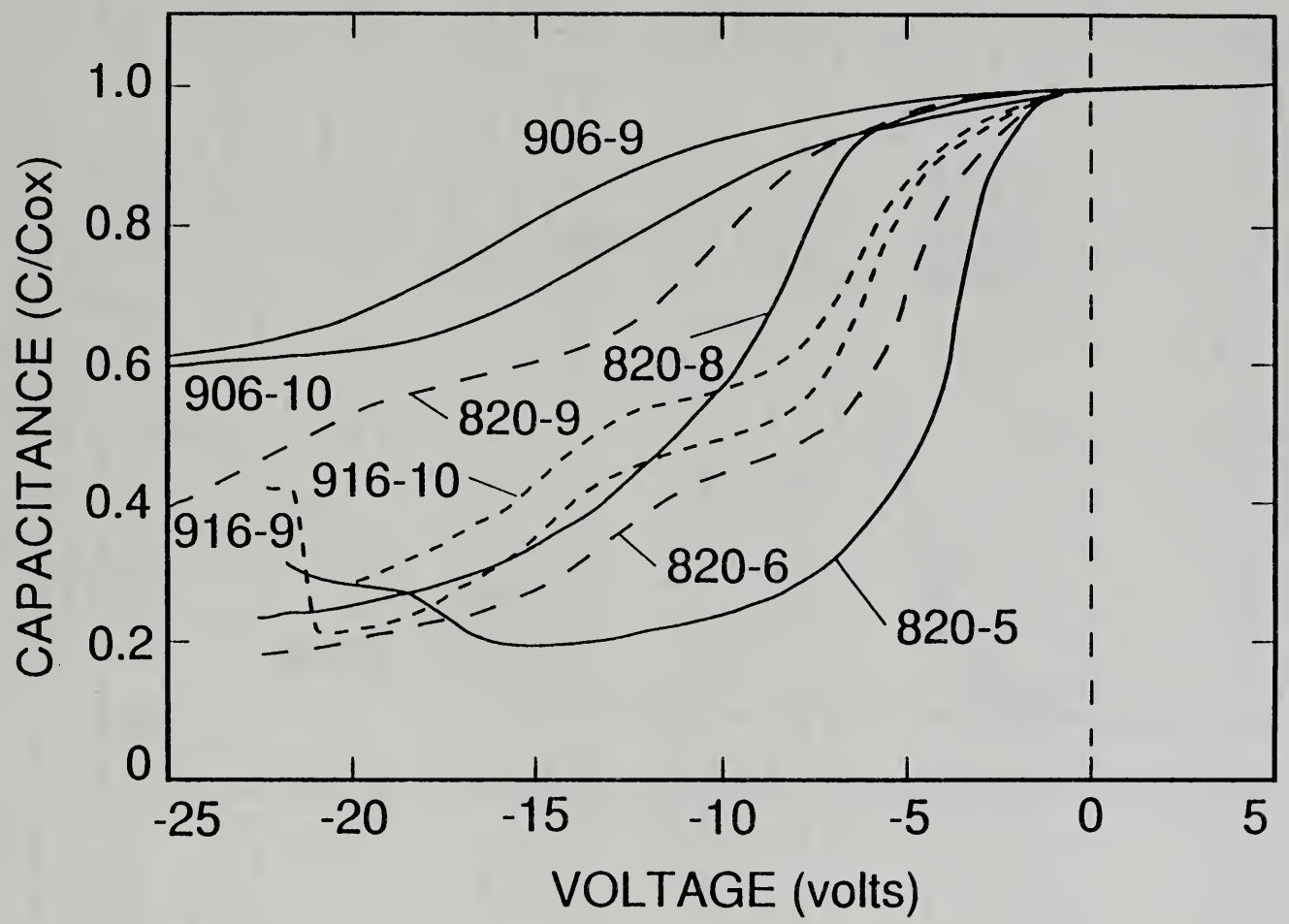

Figure 7. C-V characteristics of capacitors with CVD oxides densified in various ways, but without any post-metallization alloying. See table 1 for process information corresponding to SiC ID number.

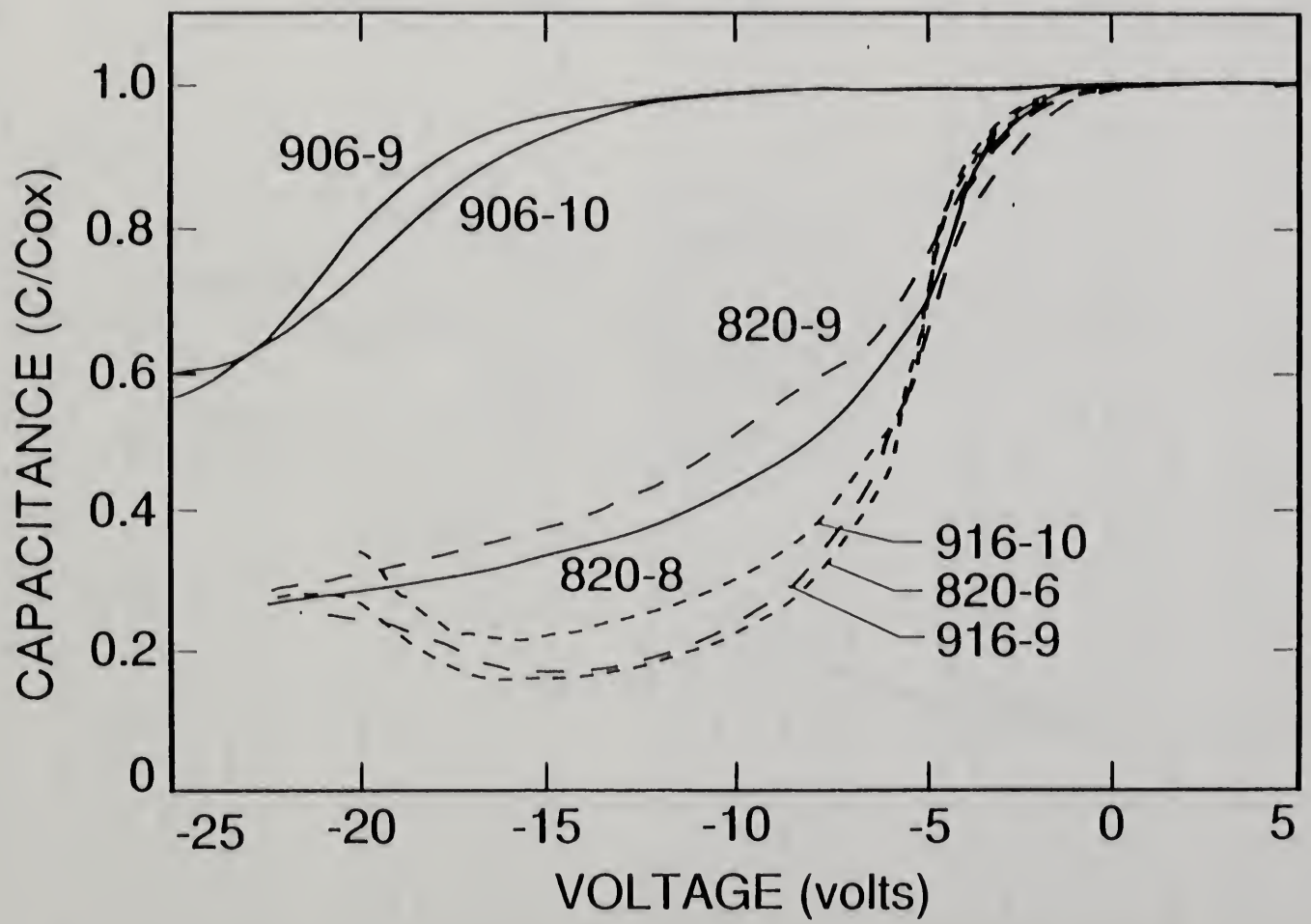

Figure 8. C-V characteristics of capacitors in figure 7 after a 450 °C forming gas alloying step. The C-V curves have been noticeably "sharpened." SiC #820-6, #919-9, and #919-10 now recover to inversion from deep depletion.

SiC #916-9 and #916-10 had higher breakdown voltages than #820-6.

From the first two batches of CVD oxide capacitors, it was apparent that a post-deposition treatment consisting of densification in nitrogen, followed immediately by a short oxidation step, followed by a post-metal alloying step, resulted in a capacitor with electric properties similar to thermal oxides. A third group of capacitors were fabricated with CVD oxides to optimize the temperature of this three-step post-deposition treatment. SiC #931-7, #931-9, #931-10, and #977-2 were given post-deposition densification and oxidation at temperatures of 900, 1000, 1100, and 1150 °C, respectively. Nitrogen densification was for 20 min at each temperature, and the subsequent wet oxidation time was adjusted for each temperature to grow approximately the same thickness of oxide.

The C-V characteristics of these four capacitors are presented in figure 9. The resulting oxide thickness after deposition and oxidation was smaller than for any of the other runs. This was due to a thinner oxide deposition than was intended. As a consequence of the thin oxide, the capacitance begins to recovery from deep depletion at smaller voltages (but about the same field) than thicker oxides. Also the inversion capacitance is a smaller fraction of the oxide capacitance.

All four of these capacitors displayed a recovery from deep depletion. The oxide fixed charge determined for these four devices ranged between about 5 and 20 x 10^{11} cm^{-2}. The oxide grown at 900 °C appeared to have the lowest fixed charge density of the group. This device, however, had a smaller breakdown voltage and had an oxide which was more conducting than any other CVD oxides. This is attributed to the relatively low densification temperature.

The peak in D_{it} observed for the thermal oxide capacitors was not as apparent in some of these CVD oxide capacitors. D_{it} at mid-gap was comparable to thermal oxides. Once properly densified and alloyed, CVD oxides were very similar to thermal oxides. The final interfacial thermal oxide appears to govern the electrical properties of the CVD oxide capacitors.

Although no advantage in electrical properties was seen in using a CVD oxide, there are possible fabrication advantages. A thick CVD oxide could be formed rapidly without consuming any of the thin SiC layer. Following densification, a thin interfacial layer of oxide could be grown, even at temperatures lower than those where a complete thermal oxide could be practically grown (about 1000 °C). These oxides will then have electrical properties comparable with those of thermal oxides which take a long time to form and which consume SiC.

By oxidizing deposited oxides, interfacial oxides grown at temperatures between 900 and 1150 °C were obtained. Combined with the thermal oxide devices, capacitors with thermal interfacial oxide grown between 900 and 1200 °C have been studied. Fixed charge was plotted against oxidation temperature, oxide thickness, or oxidation time. There is a slight trend to lower fixed charge for thicker oxides. While the 900 °C CVD oxide had the lowest fixed charge and the 1200 °C thermal oxide had the highest, oxides grown at temperatures between these extremes do not show any trend. Any

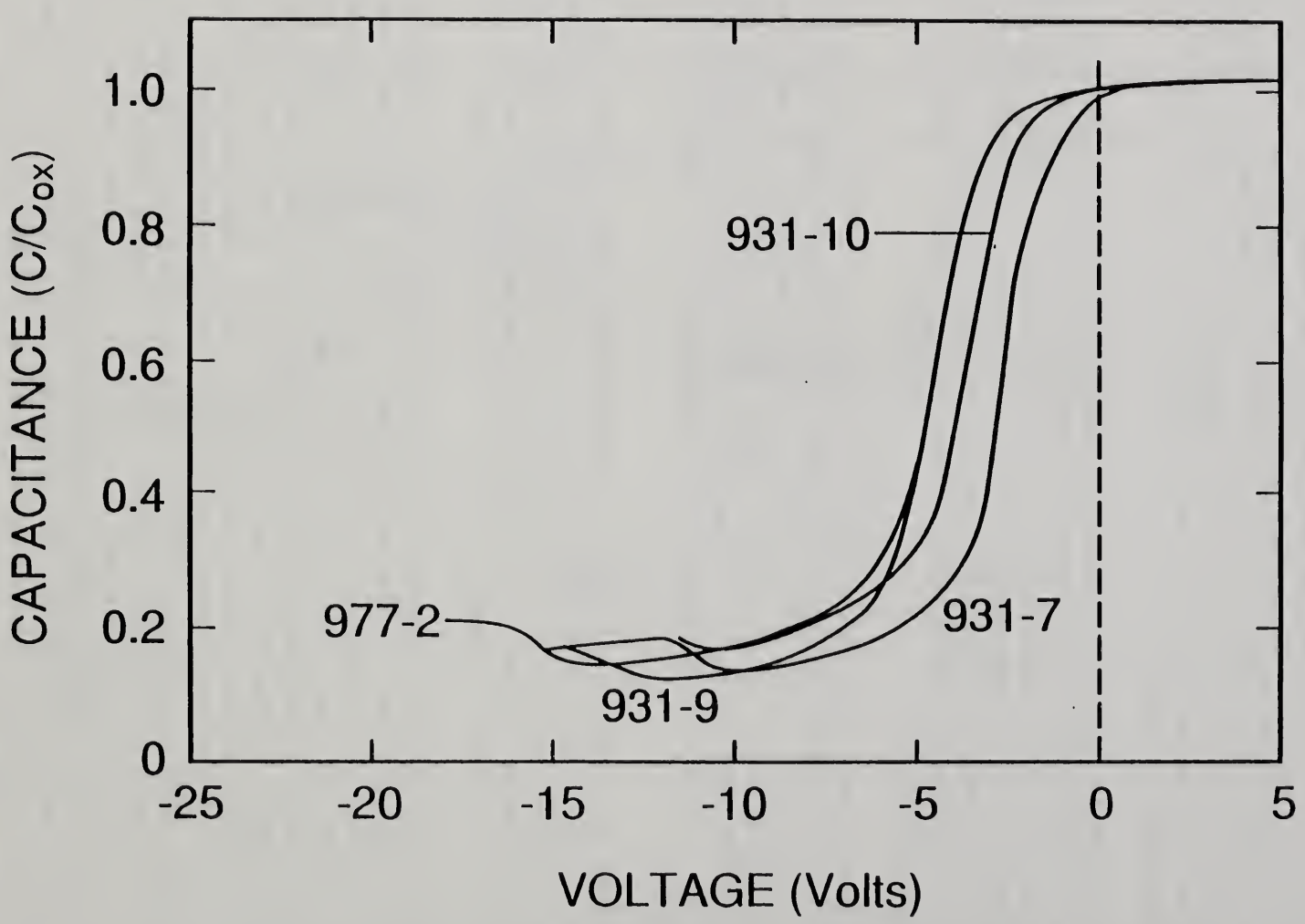

Figure 9. C-V characteristics of capacitors with CVD oxides subject densification and oxidation steps at 1000, 1050, 1100, and 1150 °C. Capacitors were alloyed at 450 °C in forming gas after metal deposition.

effect due to the oxide growth temperature is not clear.

It was apparent that the final electrical characteristics of the devices was dominated by the alloying step. The ultimate properties of the interfacial oxide could be related to the time and temperature of oxidation and the amount of carbon remaining in the oxide. Thermal oxides grown between 1050 and 1150 °C have essentially the same electrical properties. CVD oxides subject to densification and oxidation approached the quality of thermal oxides in terms of fixed and trapped charge and resistivity of the insulator. The temperature of the densification step should be at least 1000 °C to assure adequate dielectric strength.

Differences between crystals: Several subtle variations in the starting SiC material were present. An effort was made to see what effect, if any, these variations had in the electrical properties of capacitors. The C-V characteristics of capacitors fabricated on SiC covering the range of starting materials are shown in figure 10. The oxide layer for these capacitors were all grown at the same time (1100 °C in wet oxygen for 3 h). These SiC include: #919-8 (or #919-10) which were intentionally nitrogen-doped during growth, #986 which had a boron-doped (possibly p-type) epitaxial-layer, #931-6 which was grown on on-axis silicon and contained APBs, #977-6 which was grown on 1/2° off-axis silicon and did not contain APBs, and #931-5 (or #977-9) which were grown on 1° off-axis silicon and also did not contain APBs.

The greater doping of #919-8 and #919-10 are apparent from the greater inversion capacitance. Except for doping, the devices were very similar. Fixed charge and interface trap density for mid-gap levels were almost identical for all six of the different n-type materials tried. The presence of APBs did not affect the oxide charges observed with MIS capacitors. SiC containing APBs appeared to have slightly greater n-type doping density as SiC without APBs grown during the same run. This was seen for SiC from three different growth runs, #820, #931, and #975. APBs also appeared to influence the breakdown voltage of the devices. For SiC without APBs, the capacitance was usually seen to relax to a constant inversion level and not break down at fields of $>5 \times 10^6$ V/cm. SiC with APBs began the recovery from deep depletion, but the oxide often broke down at this point. This may be due to the rougher surface of the APB containing material providing sites of locally higher fields.

The boron-doped sample (#986) showed a p-type C-V characteristic. The Al (1.5% Si) contacts to this SiC were very different from those to n-type material. The equivalent resistance of the contacts was several thousand ohms compared to ten to several hundred ohms for the n-type material. The current-voltage characteristics of the contacts were slightly rectifying. The effect of the contacts is much smaller at low measurement frequencies. The C-V curve for #986 presented in figure 10 was measured at 400 Hz, compared to 1 MHz for the n-type capacitors. Much of the change in capacitance is not visible on this scale. Between -35 V and +10 V, a total change in capacitance of about 10% was observed, and flat capacitance regions corresponding to strong accumulation and inversion were observed at the appropriate voltages. Analysis of this C-V characteristic indicates that this is p-type material doped at 9.6×10^{18} cm^{-3} with a large fixed charge density, about

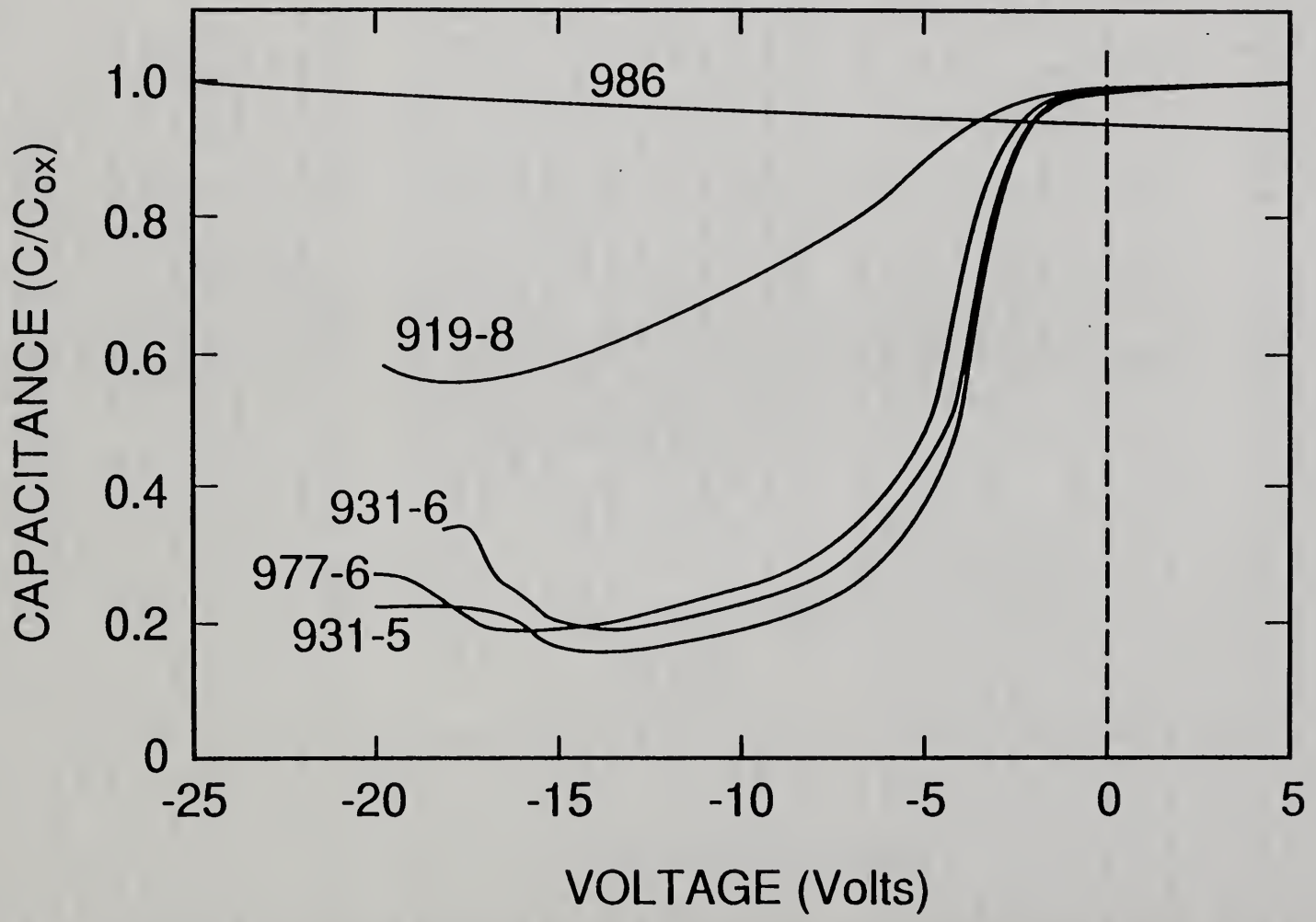

Figure 10. C-V characteristics of wet thermal oxide capacitors fabricated on SiC grown under different conditions. SiC #919-8, intentionally nitrogen doped (#919-10 is similar); #931-5 grown on 1° off-axis silicon and APB free; #931-6 grown on on-axis silicon and contains APBs; #977-6 grown on 0.5° off-axis silicon (#977-9 is similar); #986 is a B_2H_6 doped epitaxial layer.

8×10^{12} cm^{-2}.

3.5 Insulator Breakdown

The equivalent parallel conductance was monitored for all capacitors and was used to determine when the C-V characteristics were valid. Excessively large conductance would indicate a capacitor with a leaky or broken down oxide. Conductance versus voltage measurements showed a peak in the conductance, indicating the existence of fast interface states [22]. The shape of the conductance characteristic could also reveal the existence of bulk traps in the oxide.

The dielectric breakdown voltage of the oxides was determined as the voltage at which a discontinuously large current began to flow. The breakdown field is approximately this voltage divided by the insulator thickness. The current gradually increased with voltage, making the exact voltage at which the insulating layers broke down difficult to determine. The voltage at which breakdown occurred varied greatly on each sample, especially for those with CVD oxides.

For wet thermal oxides, the measured capacitance began to get "noisy" when a field of about 3×10^6 V/cm was applied across the oxide. This was usually beyond the point where the capacitance began to recover to inversion from deep depletion. A true, abrupt breakdown occurred at much larger voltages, about 6×10^6 V/cm. After breakdown, only a noisy C-V curve with a much larger parallel conductance could be measured.

Before alloying, the CVD oxide layers subject to various post-deposition treatments displayed an abrupt breakdown at a voltage slightly higher than that of some thermal oxides, about 5 to 7×10^6 V/cm. The breakdown voltage of as-deposited CVD oxide was about 5×10^6 V/cm. Sometimes after breakdown, as shown in the curves labeled 2 and 3 in figure 11, the C-V curve no longer entered deep depletion, but gradually approached a value close to the inversion capacitance.

The forward-bias breakdown voltages (capacitor in accumulation) were less than that at negative voltages. For some capacitors, especially the as-deposited CVD oxides, breakdown occurred at very small positive voltages, +1 to +3 V. The effect of this type of breakdown on the C-V behavior is also shown as curve 4 in figure 11.

4. INTERFACE TRAP DISTRIBUTIONS

4.1 Interface Trap Density Extraction from C-V Characteristics

Interface trapped charges differ from fixed charges in that they can change occupancy with gate voltage. Interface traps change occupancy by exchanging charge with the semiconductor; they interact with the conduction band by capturing or emitting electrons, and with the valence band by capturing or emitting holes. Interface traps, thus, form localized allowed states in the forbidden gap. Interface traps may differ from fixed oxide charge only in their ability to change occupancy. Charge in traps too far from the interface to exchange charge behaves exactly as if part of the fixed oxide charge.

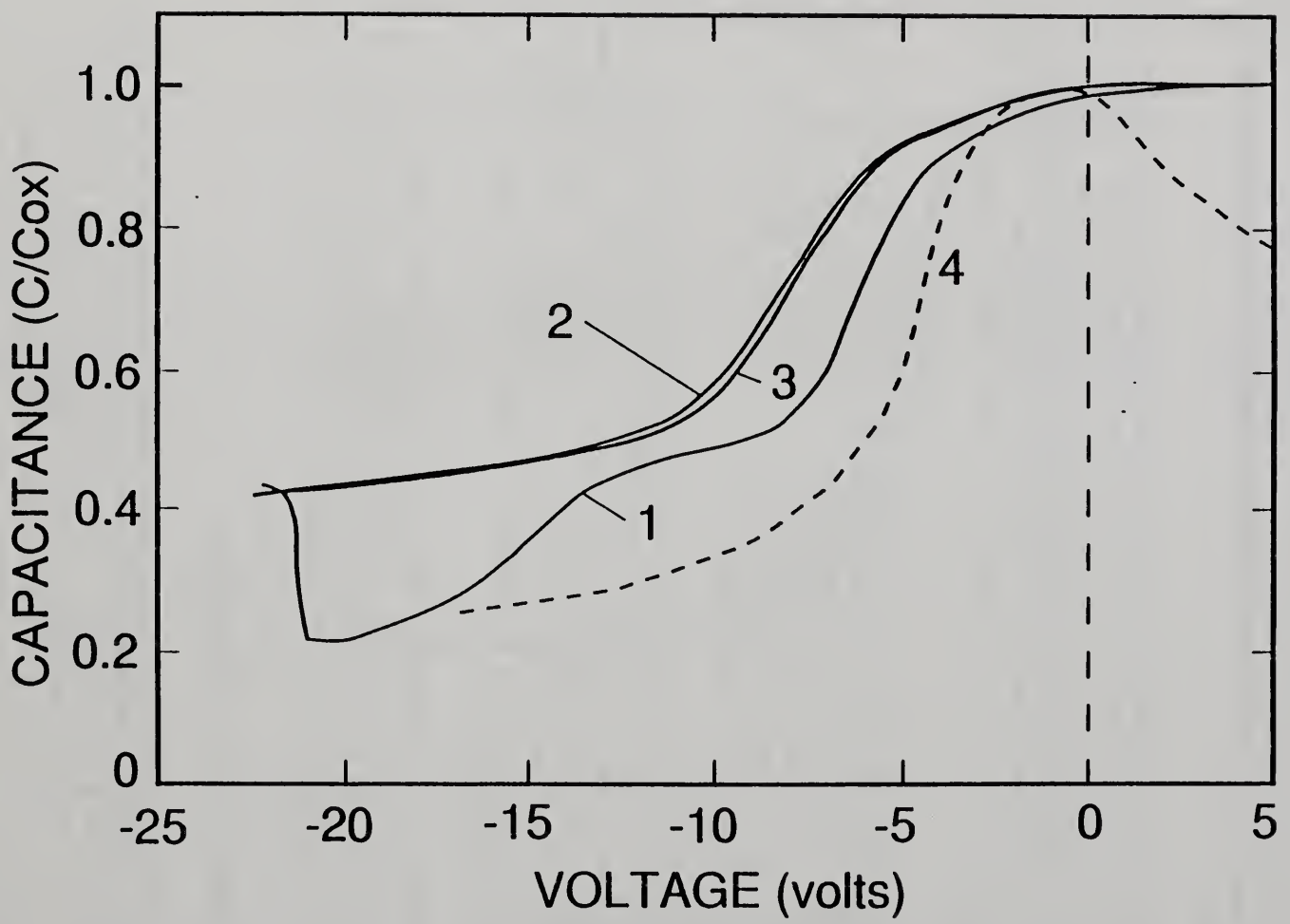

Figure 11. Breakdown behavior of capacitor with CVD oxide (#916-9). Initially, (1), the C-V curve goes into deep depletion; following breakdown, capacitance saturates at a fixed level (2) and (3). Dashed curve (4): Break down at small positive voltages displayed by some devices (#916-10).

Interface traps can be either of the donor or acceptor type. For a semiconductor in thermal equilibrium, traps of either type are filled below the Fermi level and are empty above it. In n-type material, below the Fermi level, donor-type traps are filled with an electron and are not charged, while acceptors are filled with an electron and are negatively charged. Above the Fermi level, donor-type traps have donated an electron and are positively charged, while acceptor-type traps have not accepted an electron and are not charged. Both donor and acceptor traps are at their most positive state above the Fermi level, their most negative state below.

At high frequencies, the charge states of interface traps do not follow the ac test signal, but are in equilibrium with a slowly varying dc bias voltage. They do not contribute to the measured capacitance, but rather result in a stretching out of the C-V curve with voltage. A uniform trap distribution in energy will result in a uniform stretching out of the C-V curve with gate bias. A peak in the interface trap distribution within the semiconductor band gap will result in the capacitance changing more slowly at gate voltages corresponding to the energy of the peak. It is difficult to determine if interface traps are donor or acceptors because they affect the high-frequency MIS capacitance in the same way.

Interface trap level densities are depicted in the following manner: The vertical axis is the interface trap level density, D_{it}, in units of number of charges per area distributed in energy in the semiconductor band gap (number of charges/cm^2/eV^1). This is the total number of charges and does not distinguish between donors and acceptors. The horizonal axis is the trap energy level within the band gap and is referenced from the intrinsic Fermi level, E_i. For 3C SiC, the valence band is at $-E_g/2$ (or -1.1 eV) and the conduction band edge at $+E_g/2$ (or +1.1 eV). Interface trap densities are shown in figures 15 to 17.

For this work, the interface trap density was determined using the high-frequency or Terman method [8,23]. This technique determines interface trap density by comparing the measured high-frequency C-V characteristic to the theoretical C-V characteristic corresponding to the measured substrate doping concentration and oxide thickness. The technique was chosen instead of other possibly more accurate ones because of difficulties in measuring a low-frequency C-V characteristic for SiC at room temperature.

To measure the trap density, the band gap is scanned by varying the surface potential, ψ_s, which is accomplished by varying the gate bias. The surface potential is the total amount the bands have bent at the surface from their bulk levels. Thus, the flatband voltage is at $\psi_s = 0$. D_{it} is properly positioned in the band gap by shifting the determined surface potential by the bulk potential, ϕ_b, from the intrinsic Fermi level. For an n-type capacitor being swept in voltage towards inversion, the voltage sweep causes progressively lower energies in the band gap to contribute to the capacitance.

The C-V curve is stretched out due to the interface traps changing occupancy as they are scanned across the Fermi level by the gate voltage. As the voltage sweep causes trap levels to cross to above the Fermi level, donor-type traps donate an electron and change from neutral to positive, acceptor-type

traps lose their extra electron and change from negative to neutral. The net effect is that both donor and acceptor traps change the shape of the capacitance in the same way. The Terman technique cannot differentiate between the two.

Charge neutrality requires that the charge on the capacitor gate be balanced by the semiconductor surface charge, Q_s, and the interface trap charge, Q_{it}. From Gauss's law, this is expressed as:

$$C_{ox}(V_g - \psi_s) = -Q_{it}(\psi_s) - Q_s(\psi_s). \quad (1)$$

A change in gate bias, dV_g, leads to a change in band bending, $d\psi_s$, given by:

$$C_{ox}dV_g = [C_{ox} - C_{it}(\psi_s) - C_s(\psi_s)]d\psi_s \quad (2)$$

where $C_{it} = -dQ_{it}/d\psi_s$ is the interface trap capacitance and $C_s = -dQ_s/d\psi_s$ is the semiconductor surface capacitance.

The Terman technique assumes that the substrate doping is known and uniform and that the oxide capacitance is known. The interface traps are assumed to follow high-frequency behavior. Slow dc voltage ramps were used to assure this. The MIS capacitors were also assumed to be in thermal equilibrium, that is, that the minority and majority carriers were in equilibrium. This is not true at room temperature in the dark, since even at the slowest sweep rates, the SiC capacitors entered deep depletion. The measured curves were compared to calculated deep depletion curves. In charge accumulation and depletion, the response is dominated by the majority carriers regardless of the number of minority carriers present. The possible effect of the lack of minority carriers is discussed below.

The Terman technique was applied to extract interface trap density from these SiC capacitors by the following steps [23]:

1.) The high-frequency capacitance, C_{hf}, is measured with respect to the applied gate voltage, V_g. A measured C-V curve and a corresponding theoretical C-V curve [24] are shown in figure 12. The flatband voltage shift due to the metal semiconductor work function and the fixed oxide charge is determined, and the measured capacitance curve is shifted so that C_{fb} is at $V_g = 0$.

2.) A theoretical curve of the semiconductor capacitance at high frequencies as a function of the surface potential is then computed [24]. From this, a curve of total device capacitance versus gate voltage is calculated. This is the theoretical curve plotted in figure 12. Comparing the shape of the measured curve to the theoretical one, the stretching of the capacitance at about -4 V indicates a peak in interface trap density. The shape of the C-V curve indicates an approximately uniform density of interface traps throughout the rest of the band gap.

3.) The calculated C_{hf} versus ψ_s curve is compared to the measured C_{hf} versus V_g. The ψ_s which corresponds to each V_g is determined when the capacitances are equal (figure 13). This results in a curve of ψ_s versus

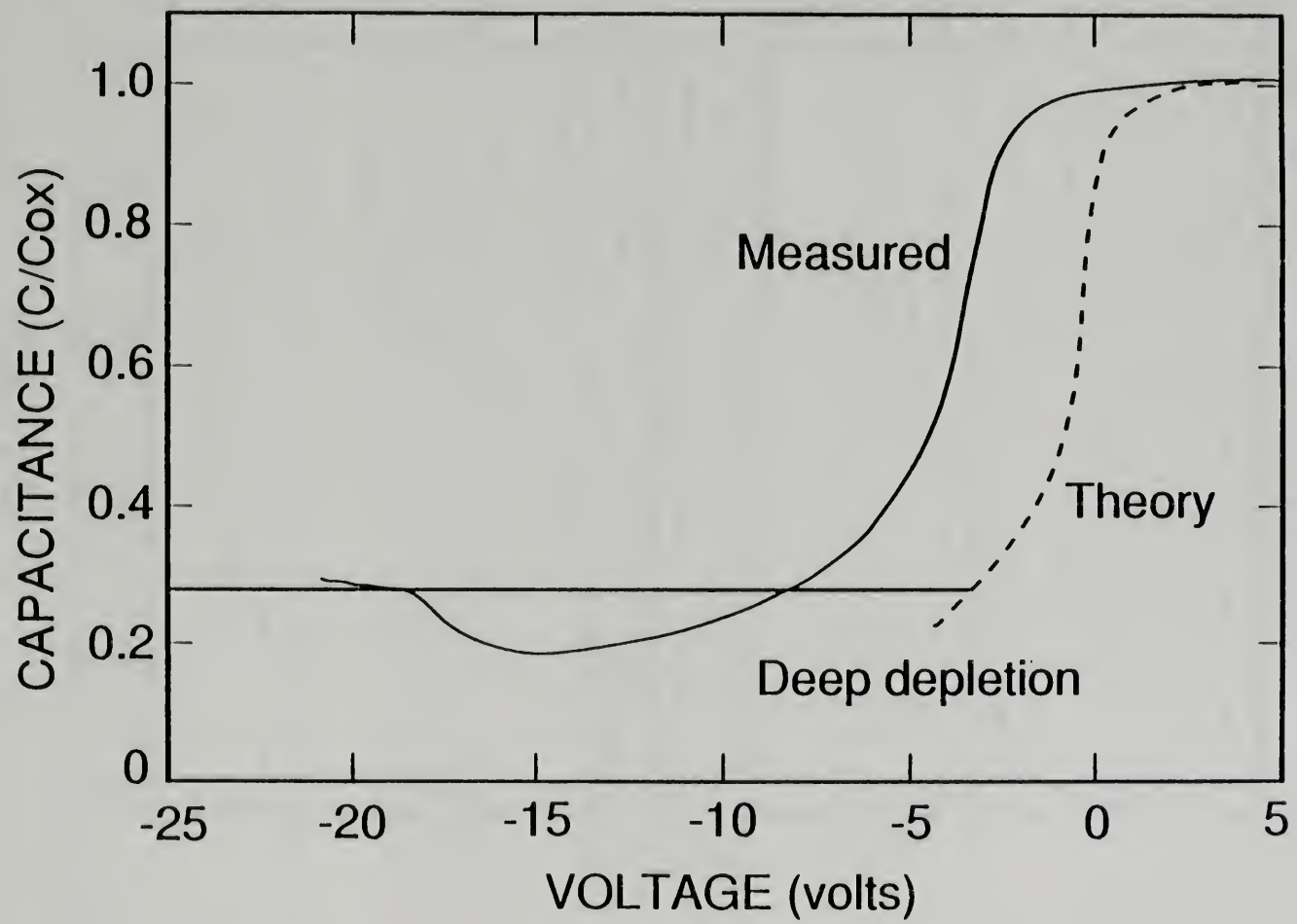

Figure 12. Measured (solid line) and theoretical (dashed line) high-frequency capacitance versus gate voltage.

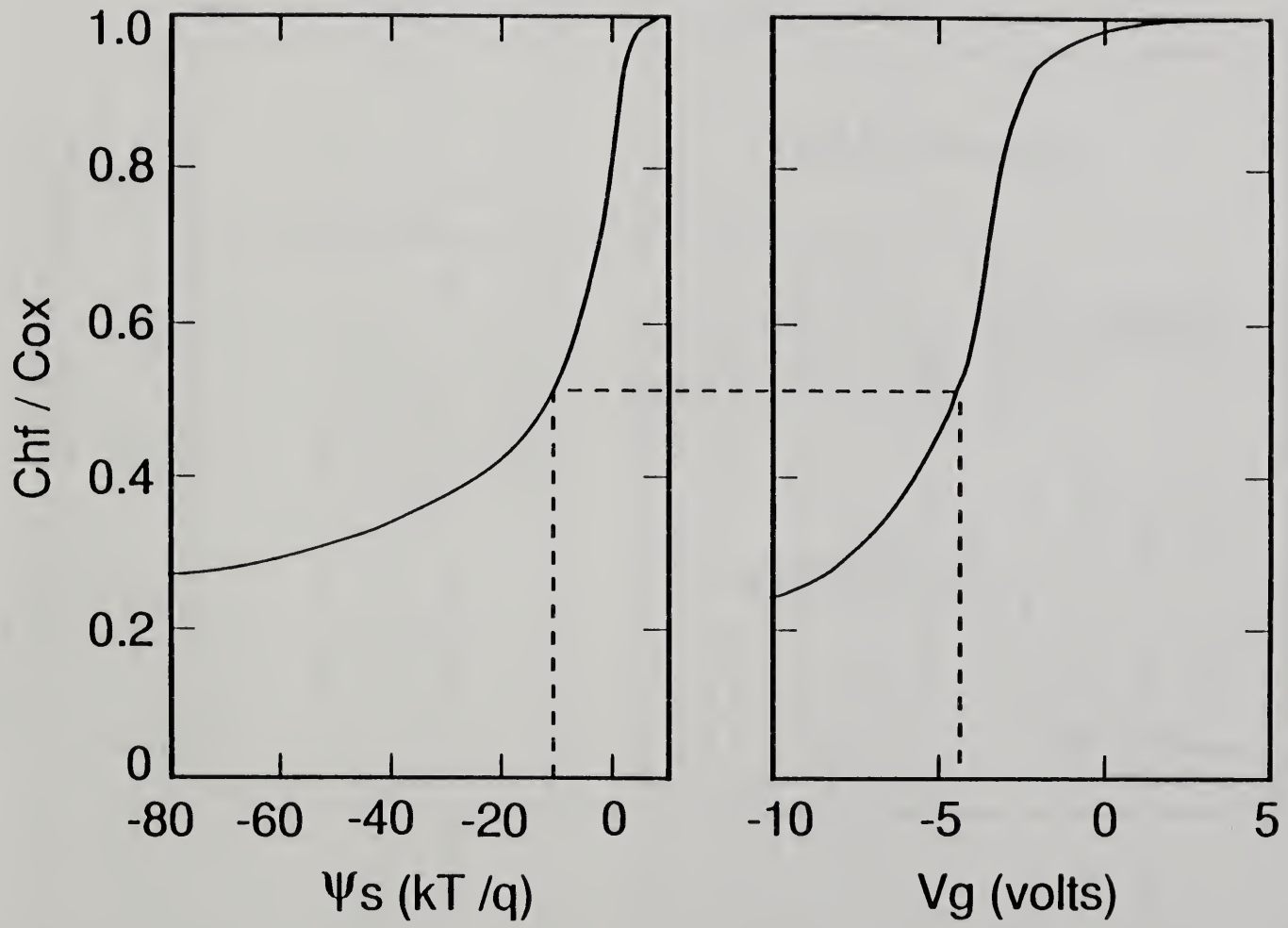

Figure 13. Theoretical C_{hf} versus ψ_s compared to measured C_{hf} versus V_g. The ψ_s corresponding to each V_g is determined when the theoretical and measured high-frequency capacitances are equal.

V_g (figure 14). This curve contains the interface trap distribution information.

4.) The interface trap capacitance, $C_{it}(\psi_s)$, is determined by numerically differentiating ψ_s versus V_g and applying eq (2). The trap density is obtained from $D_{it}(\phi_s) = (1/q)C_{it}(\psi_s)$. The resulting apparent D_{it} profile is plotted versus surface potential in figure 15.

The most obvious feature of D_{it} is the peak at about 0.6 eV below the conduction band. The location of this peak for thermal oxides varied between 0.5 and 0.7 eV below the conduction band; see figures 15 and 16. This feature of D_{it} corresponds to a flattened region of the C-V curve; that is, it is definitely due to interface traps. Most D_{it} profiles also show a second peak and an increase in density closer to the conduction band. However, the profiles are much less accurate near the band edges.

The high-frequency method has several limitations to its accuracy. The silicon band bending, ψ_s, is not directly measured, but is inferred by comparing a measured C-V characteristic to calculated C_s versus ψ_s. The calculated C_s depends on the semiconductor doping. The doping, determined from the oxide and inversion capacitances, was assumed to be uniform. There is no indication from the C-V behavior that the doping of these SiC crystals was not uniform.

Additional error may result if a true high-frequency curve was not measured. It is assumed that the interface traps are not responding to the ac signal. The difference between the 100-Hz and the 1-MHz C-V curves in figure 3 is probably due to interface traps responding to the ac. The trend with increasing measurement frequency is that interface traps do not respond much beyond 1 MHz. Interface traps are most likely to respond to the ac at gate voltages near the flatband voltage.

In accumulation, the measured capacitance approaches the oxide capacitance and limits the sensitivity with which the stretch out can be determined. A 1% change in the value used as the oxide capacitance can result in significant changes in the calculated interface trap density within a few tenths of an electron volt of the conduction band.

The lack of minority carriers in SiC in the dark at room temperature may have a significant effect in the lower half of the band gap. Interface trap profiles determined for a device at elevated temperatures or under illumination have significantly higher densities in the lower half of the band gap. The minority carrier density is not important in accumulation or depletion. The true interface trap density in the lower third of the band gap could be higher than measured. The region beyond where "strong" inversion would occur if minority carriers were present, below about -0.8 eV in the band gap, is suspect.

The profiles that have been extracted do provide a useful estimation of the shape of D_{it}. The estimate of the magnitude of the charge is less subject to error from a few eV below the conduction band edge (about +0.9 eV) to strong inversion (about -0.8 eV). More importantly, the profiles provide a relative

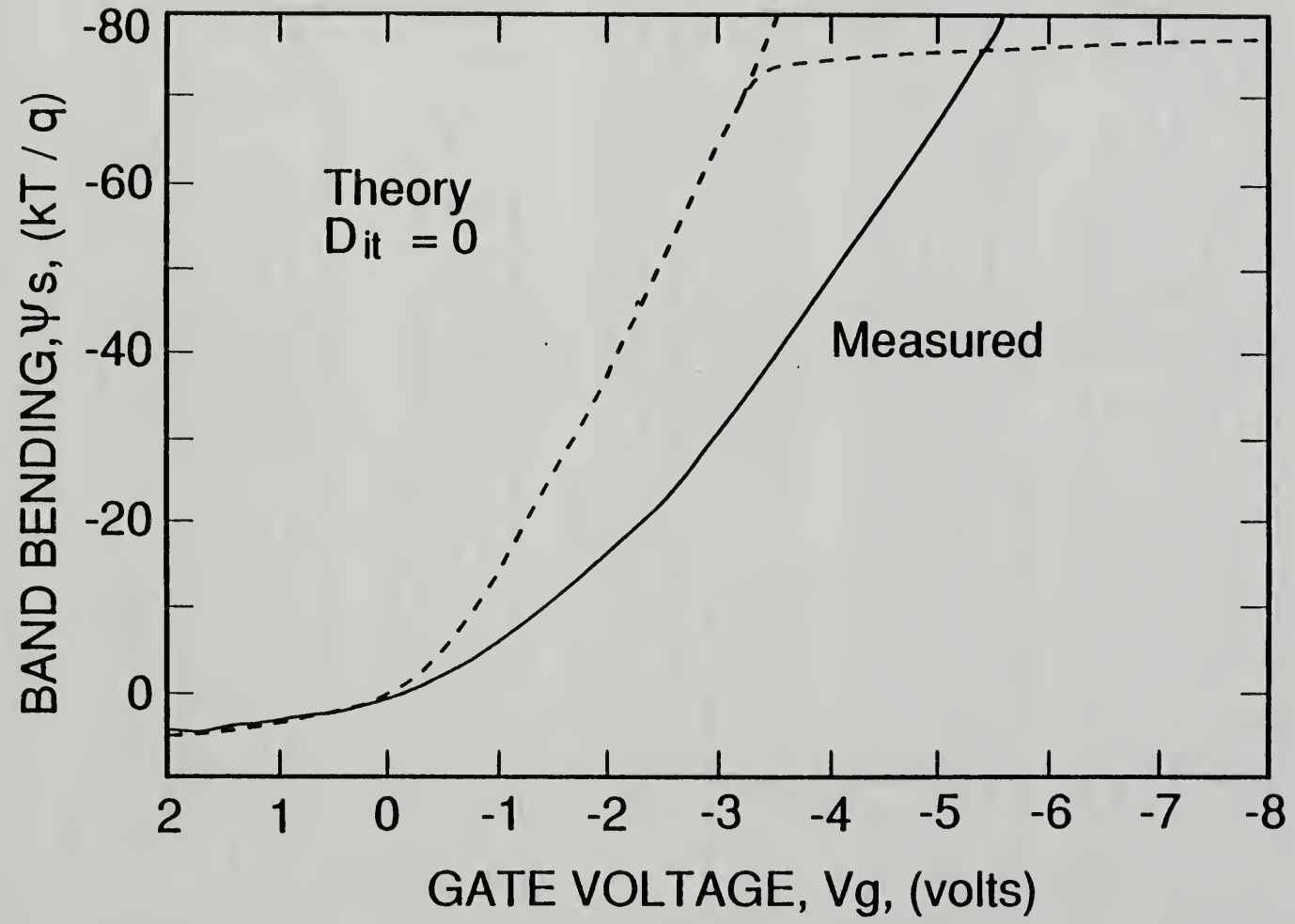

Figure 14. ψ_s versus V_g curve determined from figure 13. The dashed line is a theoretical curve with $D_{it}=0$.

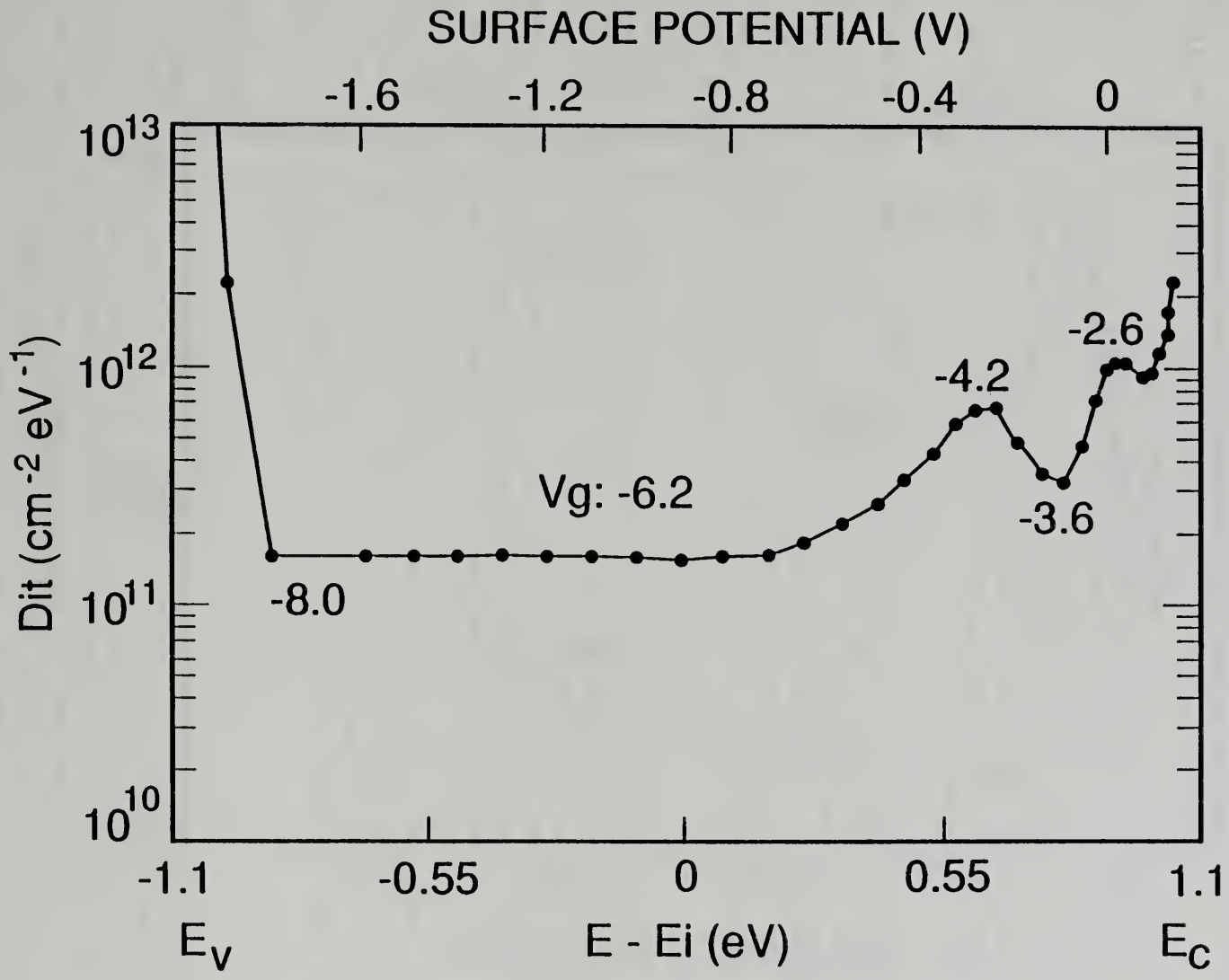

Figure 15. Interface trap level density, D_{it}, versus energy in the band gap, $E-E_i$, profile resulting from figure 14.

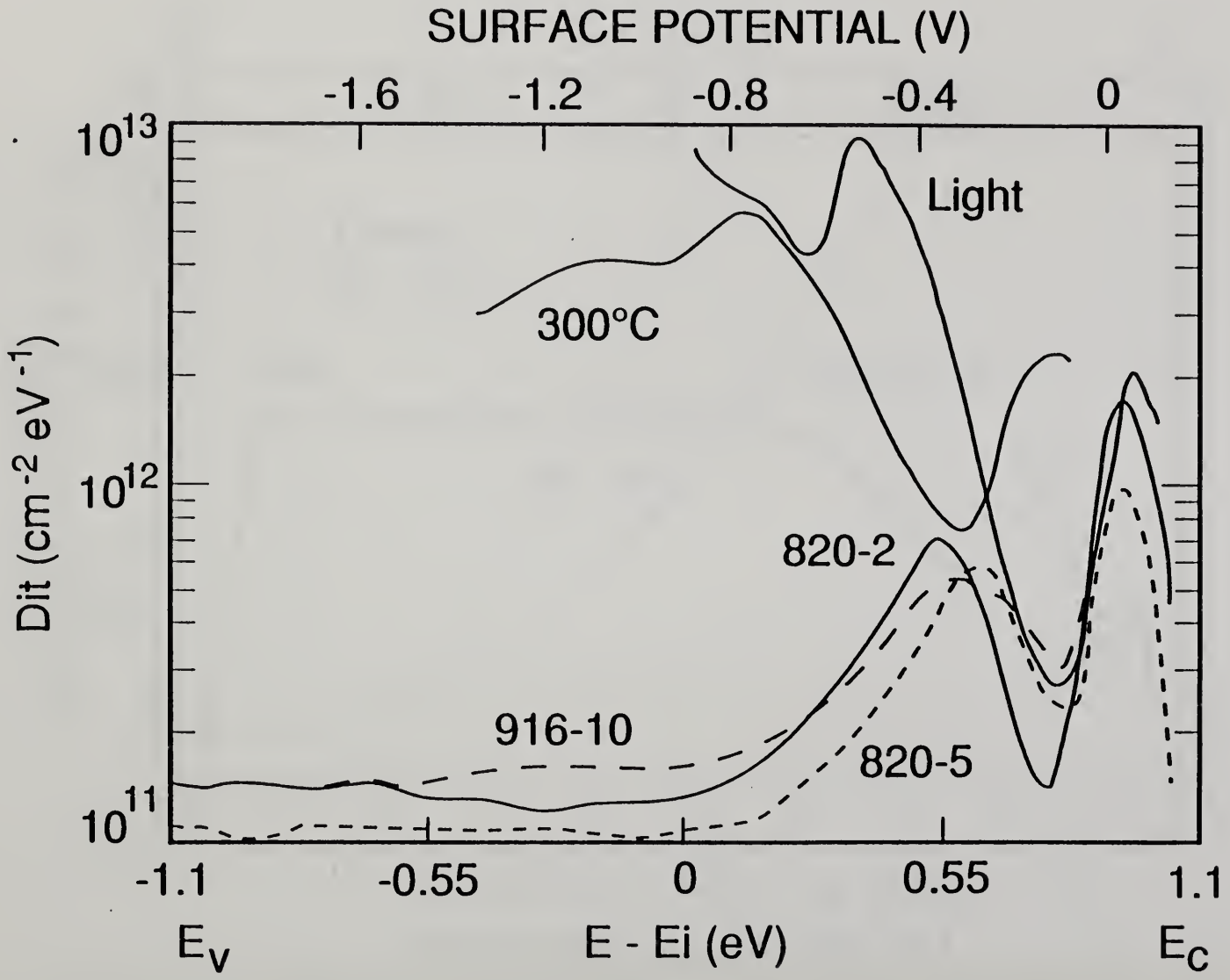

Figure 16. Interface trap density versus energy in the band gap for thermal oxide on SiC with APBs (#820-2), thermal oxide on SiC without APBs (#820-5), and densified CVD oxide on SiC without APBs (#916-10). Also shown are interface trap density extracted for #820-5 when the capacitor was illuminated and was at 300 °C.

measure of D_{it} for different processes.

4.2 Comparison of Processes

Apparent interface trap charge for SiC #820-2, #820-5, and #916-10 are shown in figure 16. These devices are, respectively, wet thermal oxide on SiC with APBs, wet thermal oxide on SiC without APBs, and densified CVD oxide on SiC without APBs. The extracted profiles are essentially identical. The presence of APBs does not seem to have a large effect on the interface trap charge. A properly densified CVD oxide has the same interface trap charge as wet thermal oxide.

Also shown in figure 16 is the interface trap density extracted from capacitors on SiC #820-5 under illumination and at 300 °C. As shown in figure 2, illumination increases the minimum capacitance. The capacitance in depletion has a gradual decrease with voltage to equilibrium. The doping concentration estimated from the inversion capacitance increases 1.5 times under illumination from the value determined in the dark. Illumination also increases the apparent D_{it} by about an order of magnitude, from the low 10^{11} to mid 10^{12} cm^{-2} eV^{-1}.

Increasing measurement temperature changes the C-V curve and the apparent interface trap density in a way similar to illumination. Values of D_{it} at mid-gap for the C-V curves in figure 4 are 0.8, 2.0, 7.0 and 20 x 10^{11} cm^{-2} eV^{-1} for temperatures of 25, 130, 200, and 305 °C, respectively. This is to be expected, as the total number of interface traps active is known to increase with temperature. The peak in the interface trap density also appears to shift towards mid gap.

The interface trap density for CVD oxides on SiC #820-9, #906-10, and #916-10, before and after alloying, are shown in figure 17. Alloying is shown to reduce the interface charge by about an order of magnitude for all three devices throughout the band gap. The summary of electrical properties for CVD processes in table 2 shows that while the trapped charge appears to decrease after alloying, the fixed charge sometimes appears to increase, due to difficulty in separating the two charge components. A capacitor with a very large trapped charge will stretch out the C-V curve, reducing the determined flatband voltage and thus the apparent fixed charge. This becomes significant above the mid-10^{11} trap range. The values of fixed charge for alloyed capacitors are closer to the true fixed charge, as the amount of stretch out due to interface traps is smaller. Fixed charge is probably always reduced somewhat by microalloying.

5. SUMMARY

MIS capacitors on SiC were fabricated using either thermal oxide or chemical-vapor-deposited oxides as the insulating layer. Wet thermal oxide was found to have much smaller oxide charge densities compared to dry thermal oxide. The effect of the wet thermal oxidation temperature (1050 to 1200 °C) on device characteristics was investigated. The growth temperature of the oxide did not appear to consistently change the final device electrical characteristics. This implies that the final post-metallization alloying step is critical for reducing MIS capacitor charge.

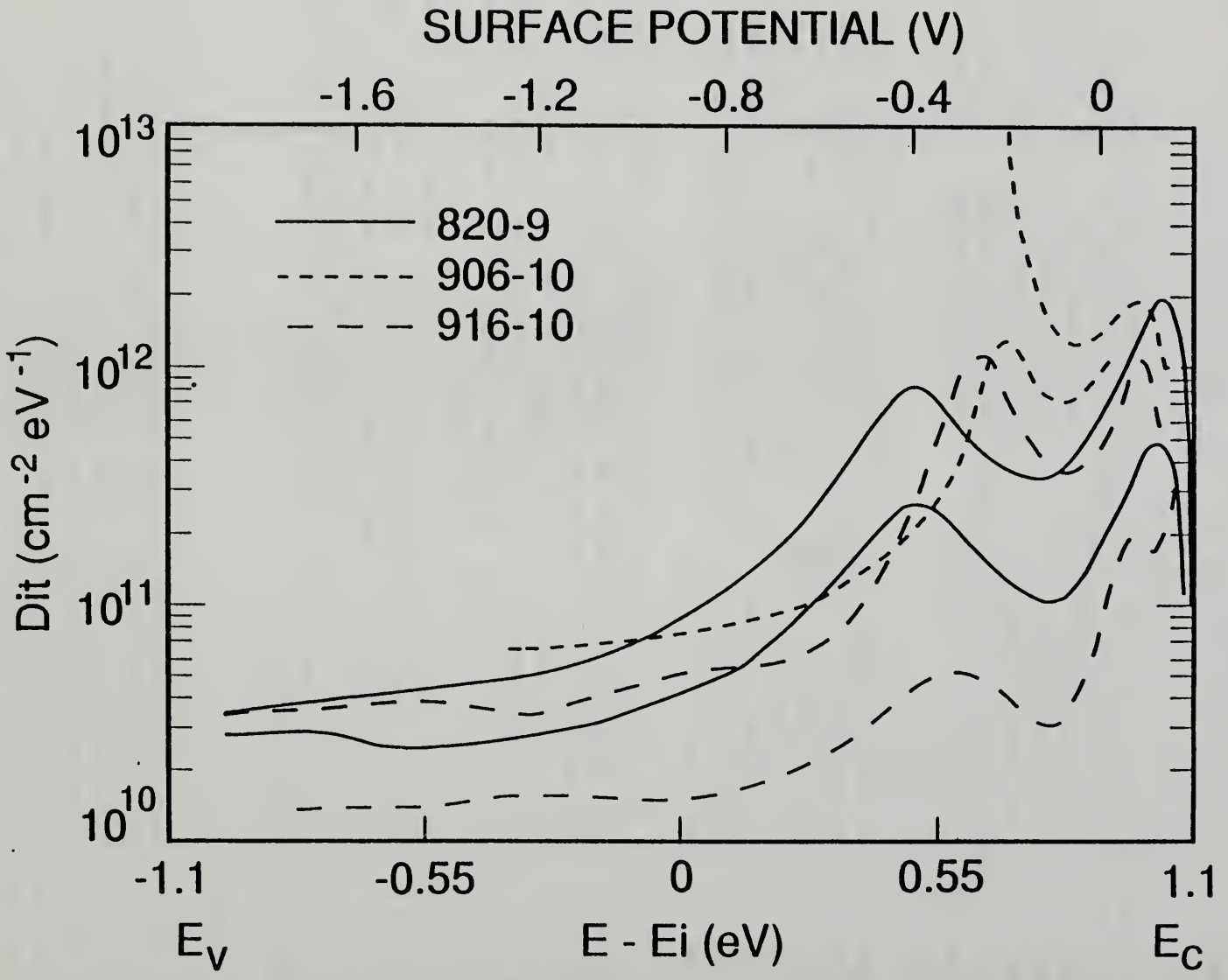

Figure 17. Interface trap density versus energy in the band gap for CVD oxides on SiC #820-9, #906-10, and #916-10, before and after a 450 °C alloying step in forming gas.

Various post-deposition thermal treatments were tried to improve the Figure 17
electrical characteristics of capacitors with CVD insulating layers. A three-step post-deposition process was found to produce the highest quality CVD oxide capacitors. This process consists of a densification step in nitrogen, followed immediately by a short wet oxidation step to grow a thermal oxide interfacial layer, and finally an alloying step in forming gas after aluminum metal deposition. A deposited oxide with approximately the same properties (fixed and trapped charges within a factor of 2) as the best thermal oxides could be formed by this process.

The improvement in electrical properties of CVD capacitors, obtained by densification and oxidation, was insensitive to the temperature at which these treatments were performed (between 1000 and 1150 °C). Below 1000 °C, the densified CVD had a noticeably lower dielectric strength and resistivity. Fixed oxide charge appeared to decrease with oxide thickness for both thermal and CVD oxides.

The MIS capacitors were characterized from their capacitance-voltage characteristics. At 1 MHz, the C-V curve displayed several distinctive features similar to that of silicon at low temperatures. At room temperature and in the dark, SiC capacitors were always observed to enter deep depletion, even at extremely low sweep rates of 0.01 mV/s. The capacitance was seen to recover from deep depletion to the equilibrium inversion capacitance when the field exceeded about 2.5×10^6 V/cm. On the reverse sweep, the capacitance displayed a stagnant inversion layer.

A small frequency dependence in the C-V curve between 100 Hz and 1 MHz was observed. This difference is due to interface states responding to the ac signal. Small flatband voltage shifts were observed following voltage stress for some capacitors. This is possibly due to charge trapping in the bulk of the oxide.

The effect of temperature on the C-V characteristics of the SiC MIS capacitor was also determined. The extent of the C-V curve in deep depletion was found to reduce as temperature increased. Above about 200 °C, an inversion layer formed during the sweep and the C-V curve no longer entered deep depletion. The apparent interface trap density was seen to increase steadily with measurement temperature up to 300 °C.

High-quality capacitors were formed by thermal oxidation at temperatures between 1050 and 1150 °C, or from CVD oxide layers densified and oxidized at temperatures between 1000 and 1150 °C. A post-metallization microalloying step in hydrogen containing forming gas was found to be critical in reducing oxide charges for either type of capacitor. Typically, for good thermal or deposited oxide capacitors, the equivalent fixed oxide charge density was in the range 5 to 9×10^{11} cm^{-2}. The interface trap level density was in the range 0.5 to 2×10^{11} cm^{-2} eV^{-1} at mid gap, with a peak of about 5 to 10×10^{11} cm^{-2} eV^{-1} at about 0.6 eV below the conduction band. Breakdown fields of the oxides were 4 to 6×10^6 V/cm, with some CVD oxides comparable to the thermal oxides. Such capacitors would be suitable for the gate insulator of an MOS field-effect transistor.

6. SUGGESTIONS FOR FURTHER WORK

There are three areas of further study that should be pursued to complete the characterization of SiC MIS capacitors. The first is continued characterization of the capacitance-voltage response of the devices. The small shifts in flatband voltage observed for some capacitors could indicate the presence of bulk oxide charge trapping. Determining the magnitude of the flatband voltage shift as a function of stress voltage and time and determining the change in equivalent parallel conductance as a function of measurement frequency would help indicate the extent that bulk oxide traps affect device behavior.

Results indicated that oxide fixed charge was a function of oxide thickness, for the examined oxide thicknesses between 400 and 800 Å. It would be interesting to examine a wider range of oxide thicknesses.

Second, the recovery of the capacitance from deep depletion to inversion is an interesting phenomenon. This could be further studied via capacitance transient measurements. The transient response of a capacitor pulsed into depletion at high temperature could also be used to estimate minority carrier lifetimes [25].

Finally, the existence of high-quality MIS capacitors on a variety of SiC crystals opens the possibility of using the devices as a tool to characterize the underlying SiC crystal. One such technique is deep-level transient spectroscopy (DLTS). It may be possible to resolve bulk trap levels in the SiC in the DLTS capacitance spectrum of MIS capacitors.

Acknowledgments

All the processing to fabricate MIS capacitors were done at the NIST Semiconductor Processing Research Laboratory. Mr. J. E. Luther and Mrs. M. L. Miller did all the processing to fabricate capacitors. Dr. G. P. Carver designed the mask set used and consulted on applying the contact resistance measurement to SiC. Drs. J. R. Lowney and M. Gaitan provided consultation and interpretations of the many MIS capacitor phenomena observed.

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Processes to fabricate metal-insulator-semiconductor (MIS) capacitors on the cubic (3C) form of silicon carbide (SiC) were studied. The insulating layers were formed from either thermally grown oxide or chemical-vapor-deposited (CVD) silicon dioxide. The effects of wet or dry oxygen and of oxidation temperatures between 1050 and 1200 °C on the electrical properties of devices with thermal oxides were determined. Various post-oxide deposition thermal treatments were investigated for CVD oxide layers. Capacitors with CVD oxide layers that were annealed in nitrogen and subject to a short wet oxidation, and alloyed after metallization, had nearly the same electrical properties as capacitors with thermal oxides. Electrical characterization techniques appropriate for these devices on SiC were developed and applied to the fabricated capacitors. The capacitors were characterized from multiple-frequency capacitance-voltage (C-V) measurements as a function of temperature from room temperature to 300 °C . The apparent interface trap level densities were estimated from the high-frequency C-V curves. The C-V characteristics of SiC MIS capacitors have several distinctive features: (1) the capacitance decreases with increasing negative voltage into deep depletion; (2) at fields of about 2.5 x 10^6 V/cm, the capacitance recovers from deep depletion to its equilibrium inversion level; and (3) on the reverse sweep, a stagnant inversion layer is seen. From the analysis of the high-frequency C-V curves, the following electrical properties of typical capacitors (both thermal and CVD oxides) were determined: equivalent fixed charge, N_f, of 5 to 9 x 10^{11} cm^{-2}; interface trap level density at mid-gap, D_{it}, of 0.5 to 2.0 x 10^{11} $cm^{-2}ev^{-1}$; and oxide breakdown fields, V_{bd}, of 4 to 6 x 10^6 V/cm.

12. KEY WORDS (Six to twelve entries; alphabetical order; capitalize only proper names; and separate key words by semicolons)

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